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VOLTAGE CONTROLLED OSCILLATOR BASED LOW SUPPLY VOLTAGE MICROBOLOMETER READOUT CIRCUIT

Ph.D. Thesis by

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ANKARA

VOLTAGE CONTROLLED OSCILLATOR BASED LOW SUPPLY VOLTAGE MICROBOLOMETER READOUT CIRCUIT

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Ph.D. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **VOLTAGE CONTROLLED OSCILLATOR BASED LOW SUPPLY VOLTAGE MICROBOLOMETER READOUT CIRCUIT** completed by **Mehmet Ali GÜLDEN** under the supervision of **Assoc. Prof. Dr. Enver ÇAVUŞ** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Doctor of Philosophy.

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July, 2021 **Mehmet Ali GÜLDEN**

VOLTAGE CONTROLLED OSCILLATOR BASED LOW SUPPLY VOLTAGE MICROBOLOMETER READOUT CIRCUIT

ABSTRACT

This thesis presents a novel, almost digital approach for microbolometer readout circuits to overcome the area and power dissipation bottlenecks of analog-based classical microbolometer circuits. A voltage-controlled oscillator (VCO) based analog-to-digital converter (ADC) is utilized instead of a capacitive transimpedance amplifier (CTIA) in classical readout circuits. This approach, which has not been reported before, produces both the required gain in the microbolometer input circuit and directly digitizes the microbolometer pixel signal. In this way, the need for large capacitances (on the order of 10- 15 pF for each column) at the CTIA circuit and voltage headroom limitation of classical microbolometer circuits are eliminated. Therefore, the proposed architecture permits to design of readout circuits with reduced pixel pitch and lower power supply, leading to higher resolution FPAs (Focal Plane Arrays) with lower power dissipation.

This study also describes a method to compensate bias heating effects for microbolometer readout circuits using a finely adjustable CMOS resistance as a reference. The proposed self-calibrated cooler-less structure dynamically modifies CMOS resistance during the integration time. This compensation structure also includes a feedback loop, which forces the oscillators to work in the linear region. The proposed self-calibration circuit is designed and simulated using a 65-nm process node and gives promising results to keep the output in the desired window up to 10K of substrate temperature changes.

A test circuit has been designed and fabricated at TSMC 65nm Multi-Project Wafer (MPW) run to validate the proposed architecture. The prototype readout IC includes a 4×4 pixel array, a 1×4 reference array, 2 VCO-based column readout, a timing generation logic, and a bias generator. The measurement results indicate that the proposed architecture can yield a gain of around 2.5 Counts/Ω. The noise of the proposed architecture is measured as 2.6 Counts. These two parameters yield a 55mK noise equivalent temperature difference (NETD), slightly above the state-of-the-art microbolometer readout circuits. The gain graphs also show that the proposed

architecture has an inherent high dynamic range (HDR) ability due to the gain non-linearity of the oscillator structure for large input voltages. In addition, the proposed architecture dissipates around $79\mu W$ power per column readout, which is almost one-third of the classical microbolometer circuits. The column readout occupies around one-tenth of the layout area of the classical microbolometer readout circuits. These two features make this architecture suitable for higher resolution lower power microbolometer readout circuits.

Keywords: uncooled thermal imaging, VCO-based sensor readout, microbolometer, readout integrated circuit, HDR operation, infrared readout circuits

GERİLİM KONTROLLÜ SALINGAÇ TABANLI DÜŞÜK KAYNAK GERİLİMLİ MİKROBOLOMETRE OKUMA DEVRESİ

ÖZ

Bu tez, analog tabanlı klasik mikrobolometre devrelerinin alan ve güç dağılımı darboğazlarının üstesinden gelmek için mikrobolometre okuma devreleri için yeni, neredeyse dijital bir yaklaşım sunar. Klasik okuma devrelerinde kapasitif transimpedans amplifikatörü (CTIA) yerine voltaj kontrollü salıngaç (VCO) tabanlı analogdan dijitale dönüştürücü (ADC) kullanılır. Daha önce rapor edilmeyen bu yaklaşım, hem mikrobolometre giriş devresi için gerekli kazancı sağlar hem de mikrobolometre piksel sinyalini doğrudan sayısallaştırılır. Önerilen mimari ile mikrobolometre devrelerinde akımın toplandığı büyük kapasitans ihtiyacı (her kolon için 10-15 pF düzeyinde) ve klasik mikrobolometre devrelerinin voltaj genlik kısıtlamalarını ortadan kaldırılmıştır. Bu nedenle, önerilen mimari, azaltılmış piksel aralığı ve daha düşük güç kaynağı ile okuma devrelerinin tasarlanmasına izin verir ve bunların her ikisi de, daha düşük güç dağılımına sahip daha yüksek çözünürlüklü FPA'lara (Odak Düzlem Dizileri) tasarlanabilmesine yol açar.

Bu çalışma ayrıca, mikrobolometre okuma devreleri için kutuplamadan dolayı ısıtma etkilerini telafi etmek için referans olarak ince ayarlanabilir CMOS direnci kullanan bir yöntemi açıklar. Önerilen kendi kendine kalibre edilmiş soğutucusuz yapı, entegrasyon süresi boyunca CMOS direncini dinamik olarak değiştirir. Bu kompanzasyon yapısı aynı zamanda osilatörleri doğrusal bölgede çalışmaya zorlayan bir geri besleme döngüsü içerir. Önerilen kendi kendini kalibrasyon devresi, 65 nm'lik bir proses düğümü kullanılarak tasarlanmış ve simüle edilmiştir. Sayısal çıkış sinyalinin 10K silicon taban sıcaklığı değişiklikleri için istenen pencerede tutulması için umut verici sonuçlar vermektedir.

Test devresi, önerilen mimariyi doğrulamak için TSMC 65nm düğümünde tasarlanmış ve Çok Projeli Yonga (MPW) üretim altyapısı kullanılarak üretilmiştir. Bu prototip okuma entegresi 4×4 piksel dizini, bir 1×4 referans dizini, 2 VCO tabanlı kolon okuma devresi, zamanlama oluşturma devresi ve kutuplama üreteci içerir. Ölçüm sonuçları, önerilen mimarinin 2,5 LSB /Ω civarında kazanç sağladığı ölçülmüştür. Önerilen mimarinin gürültüsü 2,6 LSB olarak ölçülmüştür. Bu iki parametre, son teknoloji mikrobolometre okuma devrelerinin performans olarak biraz üzerinde

olan 55mK gürültü eşdeğeri sıcaklık farkı (NETD) vermektedir. Kazanç grafikleri ayrıca, önerilen mimarinin, daha büyük giriş voltajları için osilatör yapısının doğrusal olmayışını sebebiyle doğal bir yüksek dinamik aralık (HDR) yeteneğine sahip olduğunu göstermektedir. Ek olarak, önerilen mimari, klasik mikrobolometre devrelerinin neredeyse üçte biri olan kolon başına yaklaşık $79\mu W$ güç harcamaktadır. Kolon okuma devresi, klasik mikrobolometre okuma devrelerinin yerleşim alanının yaklaşık onda birini kaplamaktadır. Bu iki özellik, bu mimariyi daha yüksek çözünürlüklü düşük güç tüketimli mikrobolometre okuma devreleri için uygun hale getirmektedir.

Anahtar Kelimeler: soğutmasız termal görüntüleme, gerilim kontrollü salıngaç tabanlı sensör okuma devresi, mikrobolometre okuma devresi, yüksek dinamik aralık, kızılötesi okuma devresi

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NOMENCLATURE

Acronyms

ADC	Analog to Digital Converter
CCO	Current Controlled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
CTIA	Capacitive TransImpedance Amplifier
DIP	Dual Inline Package
ENOB	Effective Number of Bits
FPA	Focal Plane Array
FPGA	Field Programmable Gate Array
HDR	High Dynamic Range
IC	Integrated Circuit
LSB	Least Significant Bit
MEMS	Micro ElectroMechanical Systems
MPW	Multi Project Wafer
NETD	Noise Equivalent Temperature Difference
PWM	Pulse Width Modulation
QFN	Quad Flat No lead
SNR	Signal to Noise Ratio
TSMC	Taiwan Semiconductor Manufacturing Company
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator

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CHAPTER 1

INTRODUCTION

Detecting an object without light is among the most important desires of mankind. To satisfy this need, there have been continuous research about thermal (or infrared) detectors. Thermal detectors provide clearer images in the most diverse weather conditions such as heavy darkness, fog, and smoke. Recently, thermal detector technology, originally developed for military applications, has improved dramatically and became widespread in many commercial fields from firefighting activities, perimeter surveillance to robotic vision, and building inspection [1, 2].

Infrared detectors can be mainly categorized into two groups: photonic-based (cooled), and thermal based (uncooled) [3]. Photonic-based detectors require cryogenic cooling in order to differentiate infrared related electron hole (E-H) pairs from electrically produced E-H pairs [4]. Photonically generated E-H pairs are sensed with the help of readout integrated circuits. However, there are also thermally generated E-H pairs in the material, and these thermally generated E-H pairs dominate the photonically generated E-H pairs. To decrease the thermally generated E-H pairs and to be able to differentiate the photonically generated ones, the detector should be cooled down to cryogenic temperatures (77K) [5]. Although this cooling increases the infrared imaging performance, it makes the system bigger and expensive. Therefore, these cooled detectors are mostly used in military applications, astronomical observation stations, and sophisticated medical instruments.

Thermal detectors sense the infrared radiation as an increase of temperature on the absorber material, which is which is usually implemented using a diode or a resistor in the form of a thermally isolated suspended bridge. The infrared related heat changes the absorbing materials' electrical property, the temperature sensing

device is mostly implemented with a resistor or diode [6]. The infrared related heat changes the absorbing materials' electrical property, and the change in the electrical parameters is measured by using a readout integrated circuit to generate an infrared image. Since these types of detectors do not need to be cooled, they are also named uncooled infrared detectors. Uncooled infrared detectors have attracted significant interest in military and civilian applications since they have less complexity and they are much cheaper than cryogenically cooled photon detectors [7]. Among the three of the most common uncooled detectors, namely microbolometers, thermopiles, and pyroelectric detectors; microbolometers are more favorable as they are easier to fabricate than pyroelectric detectors and they have better performances than thermopiles. With the increasing need for higher pixel counts, microbolometers are now widely adopted for most of the thermography and night vision applications in the format of focal plane arrays (FPAs) [7].

The goal of this thesis is to develop a low power and low area novel microbolometer readout circuit that enables high frame format imaging arrays. This chapter introduces the microbolometer structures. Section 1.1 summarizes the types of uncooled infrared detectors. Section 1.2 briefly mentions the physics and material of microbolometer structures and microbolometer readout design approaches. Section 1.3 mentions the products at the market. Finally, Section 1.4 presents the objectives of this thesis and reviews its organization.

1.1 Types of Uncooled Infrared Detectors

Uncooled infrared detectors can be mainly categorized into 3 categories: namely thermoelectric detectors, pyroelectric/ferromagnetic detectors, and microbolometers. This section reviews the thermoelectric and pyroelectric types of detectors, and microbolometers will be discussed in more detail in Section 1.2, as this thesis is about microbolometer readout circuits.

Figure 1.1 shows schematics of a thermocouple [8] used in thermoelectric infrared detectors. The thermocouple is made up of two thermoelectric couples with different Seebeck coefficients. Thermal heat on the junction node causes a voltage difference across the endpoints (cold points) of thermoelectric couples, and the voltage

difference across the endpoints are given as

$$V_{AB} = (\alpha_a - \alpha_b)\Delta T_{hot-cold}, \tag{1.1}$$

where α is the temperature coefficients of the junctions and $\Delta T_{hot-cold}$ is the temperature difference between hot and cold junctions. To increase the responsivity, a number of thermocouples are connected in series. This requires high pixel pitch and, as a result, lower resolution. There are thermopile type infrared imaging arrays in the market, but their use is limited due to their low performance, high pixel size (typically 100-250 μm), and low array formats (typically 8×8- 32×32).

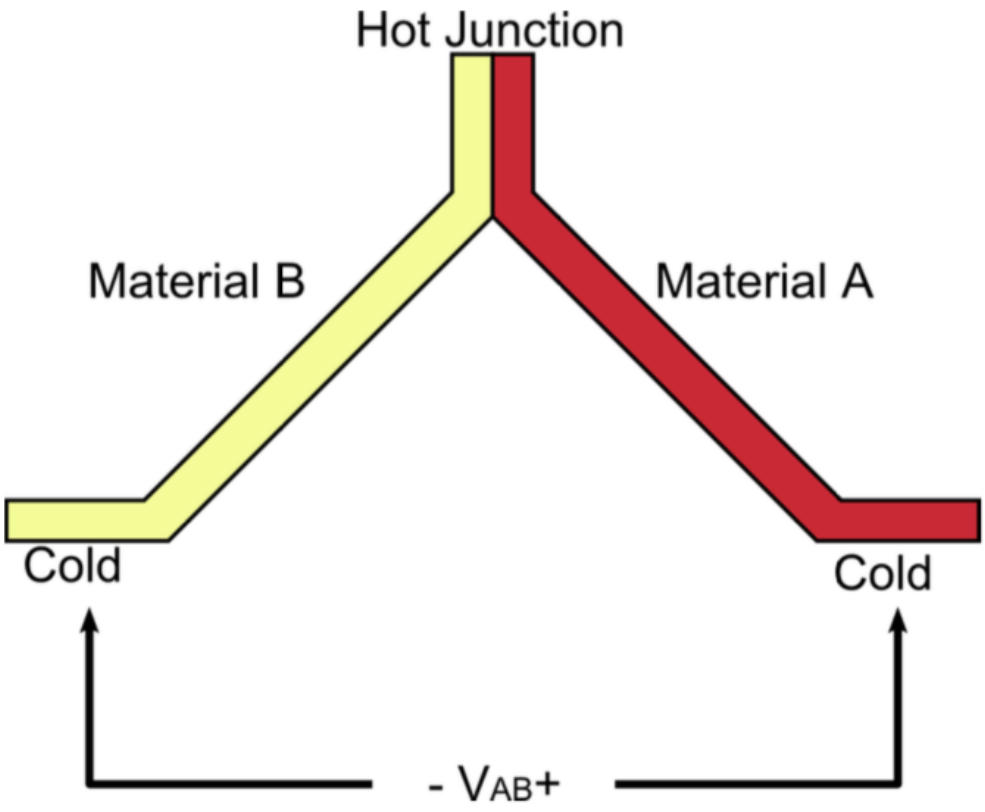

Figure 1.1 Thermocouple schematics [8] used in thermoelectric detectors

In pyroelectric thermal detectors, rapid changes of temperature results in electrical charge creation, which is named as the pyroelectric effect of the material. This excess

charge is given as [9]

$$i_d = pA\frac{\delta T}{\delta t}, \tag{1.2}$$

where i_d is the generated current, p is the pyroelectric coefficient of the material, A is the area of the electrode, T is temperature and t denotes time. As this equation states, no current is generated when the detector is exposed to constant infrared radiation. Therefore, pyroelectric detectors require implementing a chopper on top of the detector. The chopper system modulates the incoming infrared radiation and basically converts the dc infrared radiation to an AC signal modulated around chopper frequency. The peak current value is then interpreted as the infrared radiation level. However, there is one downside of the pyroelectric detectors: the pyroelectric effect of a material vanishes above the critical temperature, namely Curie temperature. For higher responsivity, pyroelectric detectors operate just below their Curie temperature level, which makes the use of thermoelectric temperature stabilizers obligatory for preventing the detector temperature to reach up to the Curie temperature [10].

Ferroelectric detectors also use the pyroelectric effect of the materials to detect thermal radiation. In ferroelectric detectors, the detector is biased to create an internal electric field, which increases the responsivity of the material. Unlike pyroelectric detectors, the Curie temperature of the ferroelectric detectors is well above room temperature, and they do not require temperature stabilizers [10]. Although ferroelectric type detectors were popular in 1990s and 320×240 FPAs with 50 μm pixel sizes were sold in high volumes, these detectors could not compete both on price and in performance with the microbolometer technology that showed impressive development with lower pixel pitch and megapixel formats.

1.2 Microbolometers

The primary type of uncooled detector is a microbolometer, a specific type of resistor or diode used to sense radiation in thermal cameras [6]. Microbolometer sensing material heats up when the infrared radiation is absorbed. This heat changes the material properties: the resistance for a resistive material or forward bias voltage

for a diode type microbolometer. Sensing materials are grown on top of the CMOS readout array. Figure 1.2 shows a perspective view of microbolometer sensing structure connecting to CMOS readout array through anchor points. Microbolometer refers to a resistive microbolometer from this point on since this thesis focuses on the design of a readout circuit for resistive microbolometers.

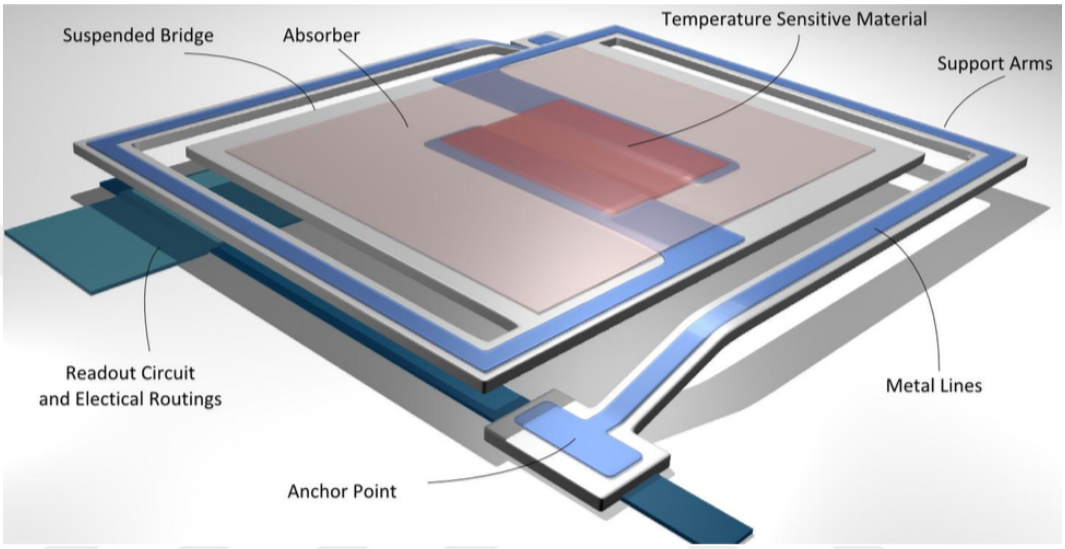

Figure 1.2 Perspective view of microbolometer sensing structure[11]

In the sensing structure of a microbolometer, thermal isolation and the quality of absorbing material is among the most important parameters. In order to increase thermal isolation between neighboring pixels, suspended bridge-like structures are used. In order to increase thermal isolation from the air, vacuum packaging is applied to every microbolometer imager. In resistive microbolometers, the sensing mechanism is the is the resistor embedded in the suspended bridge. Absorbed incident infrared radiation heats up the suspended bridge and hence the resistor resistance. The resistor resistance changes upon this thermal change. The resistance change is related to resistor's temperature coefficient of resistance (TCR) value as

$$\Delta R = R\alpha\Delta T, \tag{1.3}$$

where ΔR is the resistance change, R is the resistance, ΔT is the temperature change of the material, and α is the temperature coefficient of resistance in %/K. Since temperature change due to infrared radiation is low, the materials used as

detector resistance should have high TCR values. Resistors with high TCR materials increase the resistance difference for slight temperature changes. Different absorbing materials, such as vanadium oxide (VO_x) [12], amorphous silicon (a-Si) [5], poly silicon germanium (poly SiGe) [13] , and Yitrium Barium Copper Oxide (YBaCuO) [14] are used to increase the quality of the absorbing material. These materials have superiority and drawbacks to one another. This thesis mainly focuses on YBaCuo and VO_x type microbolometer structures.

Microbolometers are preferred for commercial and military applications due to their advantages in size, cost, and power dissipation [10, 15]. The microbolometer detectors market has been expanding and expected to grow more rapidly in the near future due to smartphone applications and night vision assistance for autonomous driving vehicles [2]. The increase in the use of microbolometers has led to a noticeable need for lower-cost thermal detectors [5, 12, 16]. One efficient way of lowering detector costs is to develop smaller and lower power readout circuits with no performance sacrifices [5]. This thesis aims to replace power and area-hungry analog blocks with digital counterparts, which requires significant architectural changes.

1.3 State-of-the-Art Microbolometers

Figure 1.3 shows the general diagram of microbolometer structure including application requirements. In this figure, label *a* shows the vacuum packaged microbolometer product, label *b*, and *c* show the pixel structure. Readout noise and readout self-heating correction capability, as well as pixel parameters, are the most important factors affecting the microbolometer performance, namely NETD (noise equivalent temperature difference) and dynamic range. MEMS (micro-electro-mechanical-systems) device parameters can be divided into thermal parameters (thermal conductance, thermal capacitance, etc.) and pixel parameters (pixel pitch, absorption coefficient, etc). This thesis aims to propose a new approach as a readout circuit that can provide the equivalent performance to the classical readout circuits with the same MEMS device parameters, which will be discussed in Chapter 2.

In worldwide, 18 companies are currently developing microbolometer imagers from low-end to high-end applications. However, 2 companies, 1 in EU (European Union)

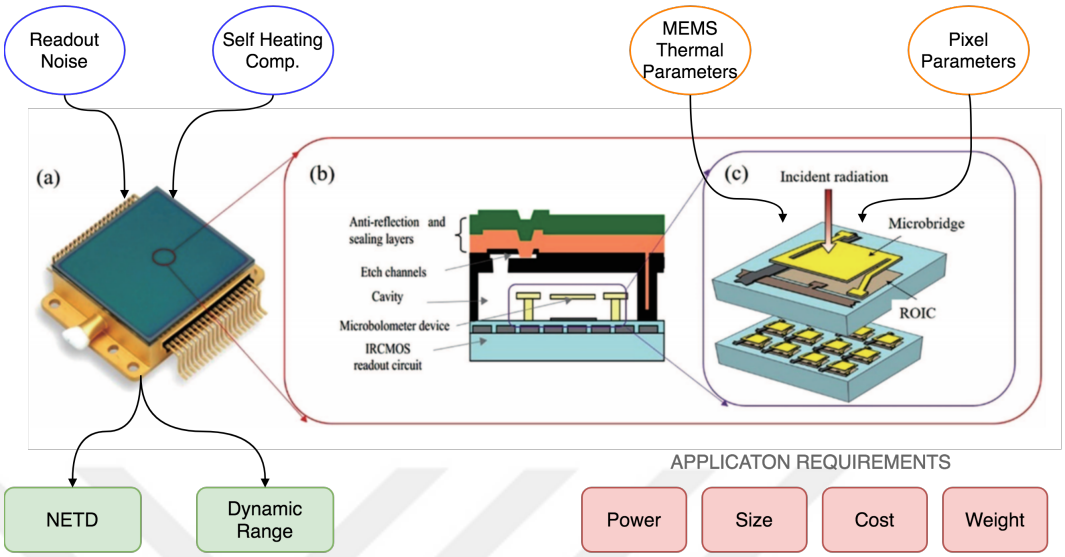

Figure 1.3 Microbolometer figure of merits and application requirements[17]

and 1 in US (United States), share the 70% of the market possess as of 2015 [2]. These companies use VO_x and a-Si as the sensing material and developed various frame format imaging arrays. The state of the art product of these two companies have 17μm and 10μm pixel pitch size with a frame format of XGA(1024$\times$768) and SXGA (1280$\times$1024) [17]. The microbolometer imaging market is currently driven with a performance of 50mK for f#1 (F-number 1) optics. This thesis aims to propose similar performance values with a new design approach.

1.4 Research Objectives and Thesis Organization

This thesis work is focused on developing novel microbolometer readout circuit, which is superior to the classical microbolometer circuit in terms of power and area. In order to obtain the advanced readout circuit, a microbolometer readout architecture is aimed to be developed with the following features;

- low power dissipation,
- compact layout area,
- digital outputs to eliminate an external ADC need,

- almost digital architecture to enable porting the design into low feature size process nodes.

In order to satisfy the above-mentioned requirements, a VCO-based microbolometer readout test circuit is designed in the scope of this thesis. VCO in this structure mainly replaces the capacitance transimpedance amplifier (CTIA) and hence decreases the area dramatically. The proposed structure also requires low supply voltages and hence reduces the power dissipation. The remainder of this thesis is organized as follows:

Chapter 2 reviews the figure of merits for microbolometers. This chapter also states microbolometer pixel parameters for VO_x type microbolometer structure for 25μm pixel pitch device in order to compare the developed readout performance with the state-of-the-art performance metrics.

Chapter 3 provides a brief information about the VCO-based ADCs and it discusses the properties of VCO-based ADCs as well as the disadvantages. This chapter also reviews the calibration structures of VCO-based ADCs.

Chapter 4 presents the proposed sensor readout circuit. This chapter gives details about the sub-blocks of the designed test circuit with the simulation results. This chapter also discusses the power and layout area reduction of the proposed architecture. Finally Chapter 4 introduces a new self-calibration algorithm to compensate the self-heating of the proposed readout architecture.

Chapter 5 describes the test setup and presents the test result of the proposed architecture. This chapter also compares test results with the classical readout architectures in literature.

Chapter 6 summarizes this thesis and concludes it by stating what should be done as future work.

CHAPTER 2

CLASSICAL MICROBOLOMETER READOUT

This chapter briefly mentions the microbolometer infrared detector performance metrics and summarizes the commonly used CTIA (charge transimpedance amplifier) based microbolometer readout circuits for resistive type microbolometers. The first section describes the performance metrics of uncooled imaging, especially microbolometers. Section 2.2 explains readout array structure and components. Section 2.3 mentions the operation principles of the classical approach, while Section 2.4 describes the fundamental problem of bias heating (self-heating) and elimination method. Finally Section 2.5 summarizes the bottlenecks of the classical readout architecture.

2.1 Performance Metrics for Microbolometers

Uncooled thermal detectors sense the infrared radiation by reading out the change in the thermal characteristics of the detecting materials. The most important performance parameters for uncooled thermal imaging are thermal sensitivity and noise equivalent temperature difference (NETD). Thermal sensitivity is defined by the temperature coefficient of resistance (TCR) value of the resistive microbolometers. NETD value shows the minimum scene temperature value that creates an output signal equals to the system's noise floor, i.e., NETD is the minimum scene temperature resolution of the imager.

The infrared radiation absorbed by the absorbing bridge heats up the microbolometer resistance. This heat changes the pixel resistance as in the following equation

$$R(T) = R_0(1 + \alpha\Delta T), \tag{2.1}$$

where R_0 is the resistance at the ambient temperature, α is the temperature coefficient of resistance, ΔT is the change in temperature. ΔT includes the heating due to infrared radiation, bias heating, and substrate temperature heating. The latter two are mostly eliminated by the readout techniques that will be defined in the last part of this chapter. However, the performance parameters are mostly determined by infrared heating. To convert the infrared related heating to the change in pixel temperature, a pixel structure thermal model is created [10]. Figure 2.1 shows the thermal model of the microbolometer structure. In this model, the thermal conductance (G_{th}) shows how well the infrared is absorbed within the pixel structure and it is defined in terms of W/K. The thermal capacitance shows that how well the pixel keeps its temperature and it is measured in terms of J/K. These two parameters together define the thermal time constant of the microbolometer structure, which defines the maximum refresh rate of the microbolometer pixel.

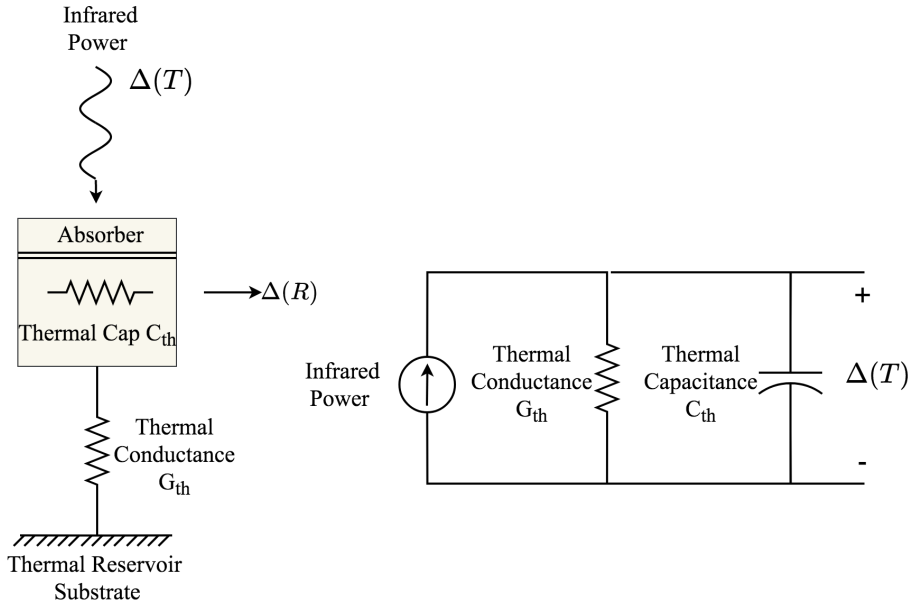

Figure 2.1 Thermal model of microbolometer pixels [10]

Temperature rise due to infrared radiation can be found by solving the model given in Figure 2.1 as

$$C_{th}\frac{d\Delta T}{\Delta t} + G_{th}\Delta T = \eta P_{ir} A_d, \tag{2.2}$$

where η is the absorption coefficient of the absorbing bridge structure, C_{th} is thermal capacitance, G_{th} is thermal conductance, and A_d is the area of the pixel structure, and P_{ir} is the Power per unit temperature in W/K. The above equation is solved for DC excitation to measure the DC responsivity of the pixel structure as

$$\Delta T = \frac{\eta P_{ir} A_d}{G_{th}}. \tag{2.3}$$

The change in pixel temperature is combined with the resistance in Equation **2.1** for a constant current bias of I_{det} in order to find the voltage change across the microbolometer resistance. The voltage change due to infrared radiation is extracted as

$$\Delta V = \Delta R I_{det} = R_0 \alpha \frac{\eta P_{ir} A_d}{G_{th}} I_{det}. \tag{2.4}$$

The voltage depends on the infrared radiation on the absorbing material. To relate this power to the scene temperature, the equation given in [10] is used. This equation states that the infrared power on the pixel structure is defined by the properties of the optics and the blackbody radiation constant as

$$P_{ir} = \frac{(\Delta P/\Delta T)_{\lambda 1-\lambda 2}}{4F^2}, \tag{2.5}$$

where $(\Delta P/\Delta T)_{\lambda 1-\lambda 2}$ is the change of power per unit area radiated by a blackbody at temperature T measured in the spectrum of $\lambda 1 - \lambda 2$, which is a constant of $2.62 W/m^2/K$ for 8-12 μm infrared band, and F is a function of distance from the optics to the target. The F-number is calculated when the target is at infinity as

$$4F^2 = 4(f/D)^2 + 1, \tag{2.6}$$

where f is the focal length, and D is the diameter of the optics. The figure of merit for measuring the performance of the uncooled microbolometers, especially microbolometers, is defined by the noise equivalent temperature difference (NETD). NETD is stated as the minimum resolvable temperature difference at the scene, which is equal to the noise floor of the microbolometer imager. NETD value for an integrated noise component of v_n can be calculated as

$$NETD = \frac{v_n}{\Delta V} = \frac{v_n G_{th}}{R_0 I_{det} \alpha \eta P_{ir} A_d}, \tag{2.7}$$

$$NETD = \frac{v_n G_{th} 4F^2}{R_0 I_{det} \alpha \eta (\Delta P/\Delta T)_{\lambda 1-\lambda 2} A_d}. \tag{2.8}$$

The performance metrics of the microbolometer readouts are mostly dependent on the noise of the readout and the thermal characteristics of the sensing material. To measure the performance metrics for the readout circuit, the noise floor is written as a parameter of NETD as

$$v_n = \frac{R_0 I_{det} \alpha \eta (\Delta P/\Delta T)_{\lambda 1-\lambda 2} A_d NETD}{G_{th} 4F^2}. \tag{2.9}$$

The voltage noise can be written in terms of bias current and the change of resistance as in Equation **2.10**.

$$v_n = I_{det} \Delta Rpixel \tag{2.10}$$

The noise of the readout consists of 2 main factors: the electrical noise of the detecting material and the noise sources of the readout electronics. When the readout circuit noise floor is below the noise of the detecting material, the NETD value can be derived in terms of the resistance value of the readout circuit. The change in resistance as a parameter of NETD can be written when Equation **2.9** and Equation **2.10** are combined as

$$\Delta R_{pixel} = \frac{R_0 \alpha \eta (\Delta P/\Delta T)_{\lambda 1-\lambda 2} A_d NETD}{G_{th} 4F^2}. \tag{2.11}$$

To quantify the performance parameters in terms of the resistance value, typical microbolometer parameters for 25μm pixel pitch are used. Table 2.1 shows the typical thermal and electrical parameter values for 25-μm pixel pitch YBaCuO or VO_x type microbolometer resistor with 60 kΩ nominal value [18]. When these parameters are applied to Equation **2.11**, a 0.9 Ω of resistance change results in 50mK NETD value. This means that the proposed readout architecture should sense a resistance change of 0.9 Ω in order to compete with the state of the art microbolometer readout circuits [16, 19, 20] while keeping the noise floor of the electronics below the electrical noise of 0.9 Ω.

Table 2.1 Parameter values for typical microbolometer readout

Symbol	Name	Value
R	Nominal Resistance Value	60 kΩ
PP	Pixel Pitch	25 μm
FF	Fill Factor	0.9
η	Absorption Coefficient of the Pixel	0.6
G_{th}	Thermal conductance of the pixel resistance	20 nW/K
f#	F-number of the optics	1
α	TCR = Temperature coefficient of resistance	0.03 %
ΔR	Resistance Change due to 50mK temperature change	0.9 Ω

2.2 Readout Array Structure

Classical microbolometer readout architecture, a block diagram is given in Figure 2.2, consists of the pixel array, reference pixel array, vertical row selection, and output multiplexing circuits, digital controller, and bias generator.

Bias generator generally implements bandgap reference circuits in order to create temperature and supply independent bias voltages and currents for the readout integrated circuit. Another key function of the bias generator is to supply low noise voltages for the pixel and reference detectors. These voltages are designed so as to cancel out their common-mode noise components at the pixel biasing structure.

Digital controller constitutes of a memory, a timing engine, and a programming interface. The programming interface is used to configure the memory array through

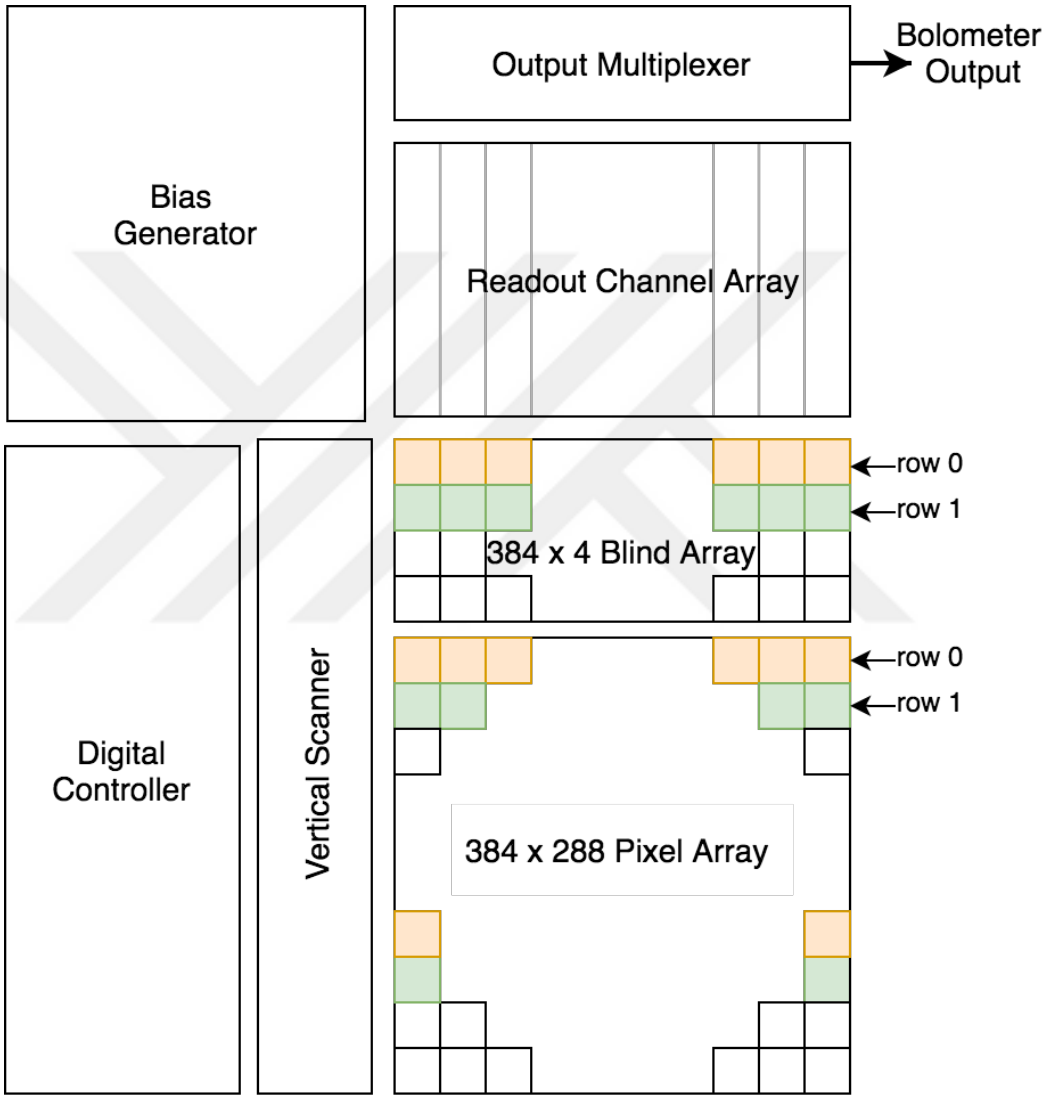

Figure 2.2 A classical microbolometer imager bock diagram

an SPI or an I2C buses. The register based memory defines the configuration of the readout circuit, such as image size, gain, etc., and holds the programmable bias values. The timing generation logic generates the row synchronization and the frame synchronization signals as well as the internal column readout circuit signals.

Microbolometer readout circuits operate in a rolling line structure, which means rows of the imaging array are red-out consecutively. The vertical scanner selects one row at a time for both active and blind pixel arrays. Some of the blind pixel arrays are shared across the pixel array. This sharing is also carried out at the vertical row selection circuit. Output multiplexing circuit simply multiplexes column readout outputs one by one to the bolometer output port.

The readout channel mainly amplifies the infrared related pixel current/voltage. Since this thesis focuses on the readout circuits, the readout approach of the classical readout circuit will be presented, and the details will be investigated in the next section.

2.3 CTIA Based Readout Architecture

The analog signal chain of the CTIA based microbolometer readout consists of 2 parts: pixel bias, and integration. Figure 2.3 shows the schematics of this architecture. Pixel bias structure includes voltage biased active and blind microbolometer pixels. Active pixel responds to the heating effects due to infrared radiation and biasing, yet the blind pixel responds to only bias heating. As the temperature increases on the active bolometer pixel due to infrared radiation, the resistance decreases. Hence, the current flowing through the lower part of the pixel biasing node increases. The CTIA circuit amplifies this excess current with the gain defined as integration time over integration capacitance. The charge on the integration capacitance is removed with a reset operation in order to start the integration from a known state, i.e., before enabling the current flow through active and blind microbolometer pixels.

The integration time is kept as high as possible for two reasons: decreasing the bandwidth of the pixel circuit (hence decreasing the integrated noise at the input stage) and increasing the integrator's gain. However, increasing the integration time

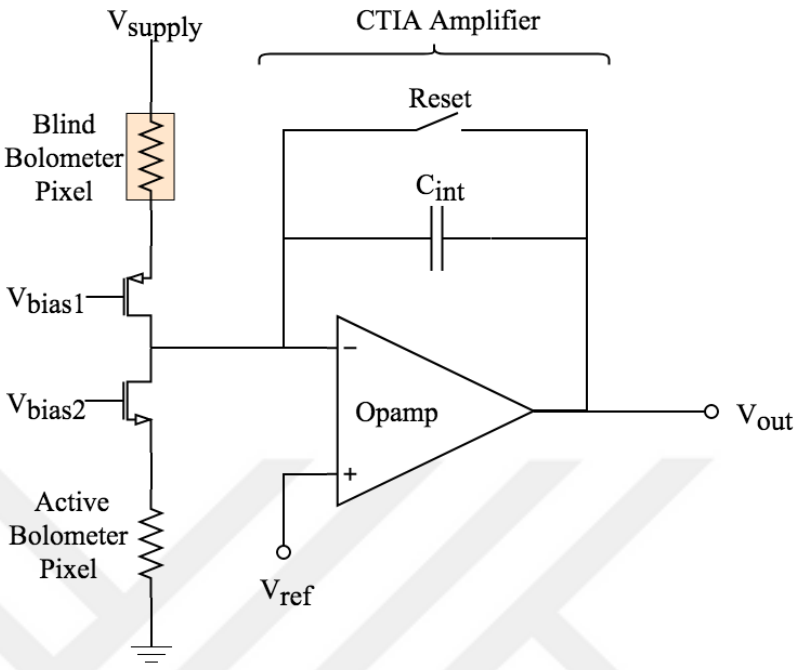

Figure 2.3 CTIA based microbolometer readout architecture

increases the row time of the readout, and this results in an increase of frame time and hence a decrease in the frame rate. Besides, increasing the gain of the CTIA integrator circuit decreases the dynamic range of the microbolometer readout circuit, as the voltage headroom is limited. On the order of 10-20 pF, huge integration capacitances are generally implemented in the microbolometer readout circuit to decrease CTIA gain and hence increase the dynamic range of the microbolometer. Therefore, classical column readout circuit designs yield a large layout area. Large capacitances occupy a significant percentage of the column readout layout area, and this percentage increases with decreasing pixel pitch. As the pixel pitch and hence the column readout pitch decreases, the CTIA integration capacitor area becomes a significant bottleneck in designing large format microbolometer readout circuits. For example, in a readout circuit with 25-μm pixel pitch, the column readout circuit area to the pixel area is about 0.5 [19]. However, the same ratio becomes approximately 0.75 for the 12-μm pixel pitch design of the same product [21]. One of the goals of this thesis to eliminate the need for a large layout area.

The classical microbolometer readout technique dictates to use of supply voltages

bigger than 3.3V as the active and blind pixels are connected in series. This high supply voltage becomes another bottleneck of the classical microbolometer readout circuits. The column readout circuit also requires high supply voltages to increase the dynamic range of the system. Both of these requirements make the classical microbolometer readout circuits power-hungry. As a result, this increases the power dissipation. For instance, using a 3.3-V supply voltage and the same 640 $\times$ 480 FPA size, two recent readout circuit implementations dissipate 150 mW [22] and 100 mW [19] in analog video output mode. Also, 350mW power consumption is reported in [22] the digital output mode with an on-chip 12.5 ENOB ADC structure. Due to this large area and high power supply problems of classical microbolometer readout circuits, implementations with image formats larger than 1024 $\times$ 768, or pixel pitch smaller than 10 μm [23] and supply voltage less than 3.3V are not reported in the literature. Another aim of this thesis is to enable large-format arrays with small pixel pitch values.

2.4 Self-Heating and Elimination Method

Microbolometer pixel resistances should be biased to measure resistance change due to infrared radiation. Biasing also creates power on the absorbing bridge structure and, hence a temperature increase on the pixel resistor. This phenomenon is called self-heating or bias-heating. Several offset correction design methods are proposed to eliminate the effect of the resistance changes caused by self-heating [24–26]. In a classical microbolometer readout architecture (Figure 2.3), a row of the blind (reference) microbolometer resistors, unaffected by incoming incident radiation, is used to calibrate the self-heating effect. This method requires that the active pixel and reference pixel's thermal parameters be exactly matched to cancel out the self-heating effects altogether. This means that the number of reference pixels should be equal to the number of active pixels in the imager. However, this is not be possible due to size limitations.

Microbolometers require a rolling line type of imaging as their nature dictates. The rolling line of imaging means that the rows in one frame are integrated and amplified consecutively, as shown in Figure 2.2. The reference resistors are shared across the

frame for self-heating cancellation due to size constraints. This requires designing a reference pixel that will heat almost the same amount as the biasing. The work in [27] states that the thermal capacitances of the reference pixel should be equal to the thermal capacitance of the active pixel when the integration time is far shorter than the time constant of the pixel. The sharing of reference pixels creates another issue that the reference pixels should cool down faster than the active pixels, which results in a higher thermal conductance value than that of active pixel [27].

To model temperature changes on a single pixel, a Matlab Simulink model, as in [28], has been created with the parameters given in Table 2.1. Figure 2.4 shows the Matlab Simulink model of the single-pixel structure. The thermal model of the microbolometer structure, green area in the figure, implements the heat balance equation. The ground temperature of the heat balance equation is connected to the substrate temperature, labeled as $T_{substrate}$, to model the effect of substrate temperature on the output. This substrate temperature defines the initial resistance of the microbolometer pixel. To take the impact of scene temperature, labeled as ΔT_{scene} in the figure, into account, electrical, thermal, and system parameters of the microbolometer structure are modeled in the red area. This red section converts the scene temperature into electrical power, which results in a temperature change on the pixel structure. The output of the heat balance equation in this model is the pixel temperature, T_{pixel}, and change in the pixel temperature, ΔT_{pixel}. The pixel temperature is fedback to the electrical model of the resistor, which outputs the pixel electrical power due to biasing.

This model is run with a 1 ns time steps to make this model as accurate as possible. At each time step, the electrical power due to resistance change and the resistance change due to electrical energy are calculated and forwarded to each other. Figure 2.5 shows the pixel temperature and resistance change during the integration period. The pixel temperature increases almost 8 K, which decreases the pixel resistance by 8k Ω with the biasing. Therefore, the cancellation of the self-heating effect is paramount for microbolometer readout architectures.

The electrical model of the resistor supports current bias and voltage bias options to use the system to model for both the classical approach and the new approaches.

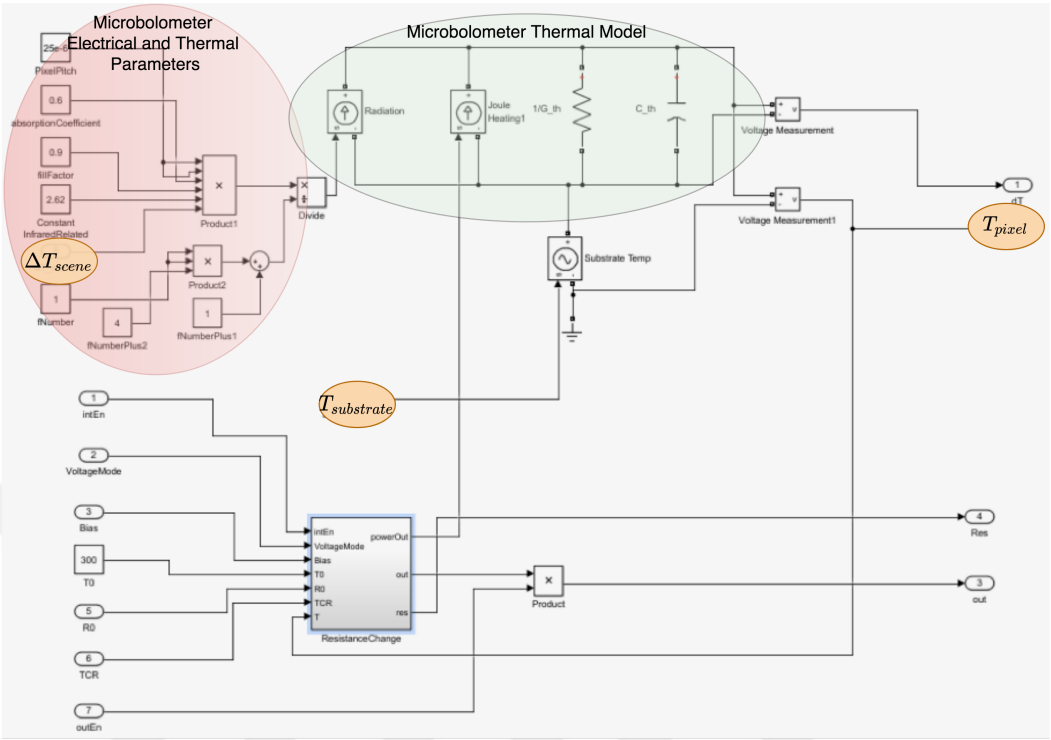

Figure 2.4 Single Pixel Matlab simulink model

Besides, the electrical model also includes integration enable and output enable options. The integration-enable option models the change of the pixel temperature and resistance only during the integration. The integration-enable feature is used to model the sharing of reference resistors in one frame capture. The output-enable property is also used for reference resistances to match the output current of a unique pixel with the active resistance. Figure 2.6 shows the active pixel resistor's and reference resistor's temperature change of classical microbolometer readout circuits during the frame capture. The cooling curve of the reference pixel is faster than that of the active pixel since its thermal conductance parameter is higher.

The electrical and thermal parameters of active pixel and reference resistors are not precisely matched due to imaging array size constraints. This causes the microbolometer output voltage to drift for slight substrate temperature changes. A new Simulink model, in Figure 2.7, includes active pixel model, reference model, and CTIA type integrator to model the effect of substrate temperature on the integrator output. Voltage-biased active pixel and reference resistors create current outputs.

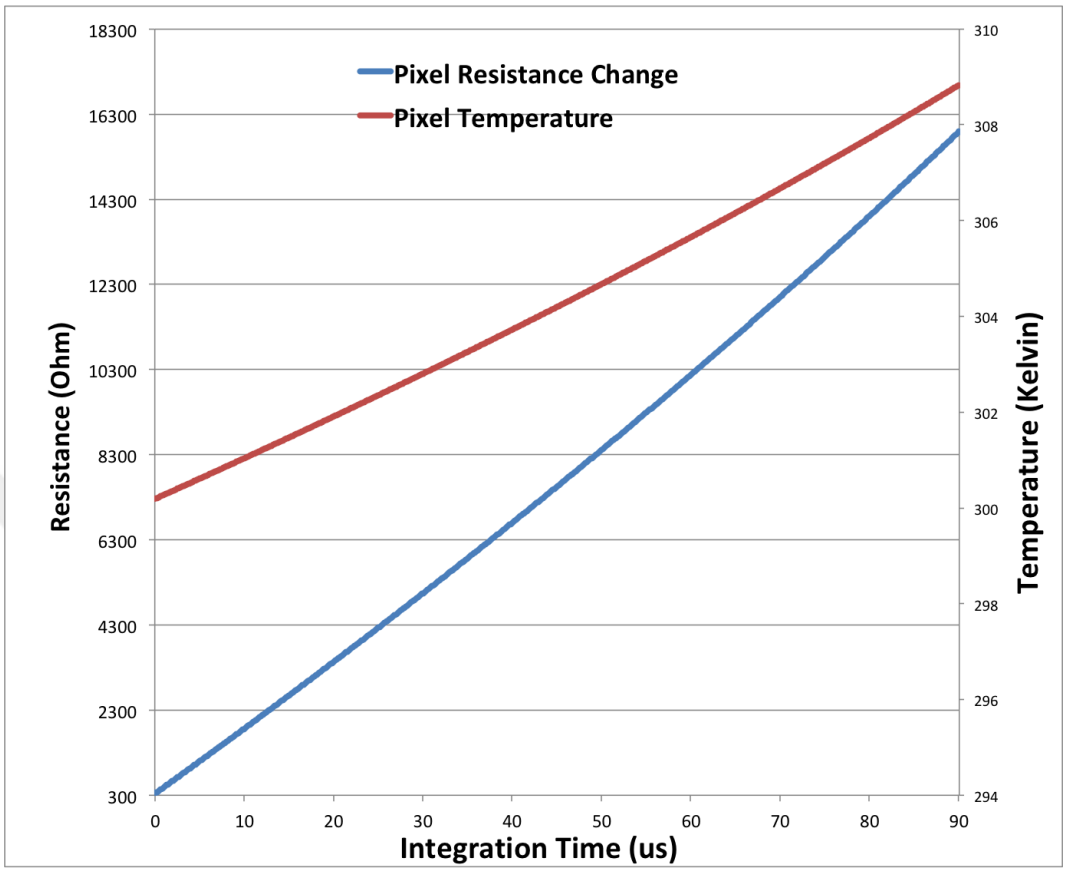

Figure 2.5 Pixel resistance and temperature change with bias

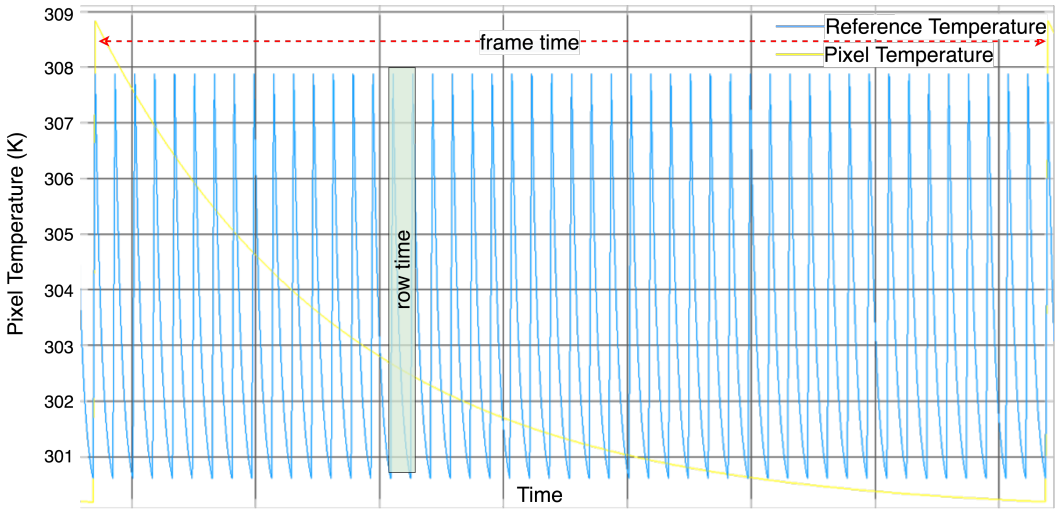

Figure 2.6 Pixel and reference resistance temperature change in one frame capture

CTIA integrator amplifies the current difference between active and reference pixels with a capacitance of 15 pF and an integration time of 90 μs.

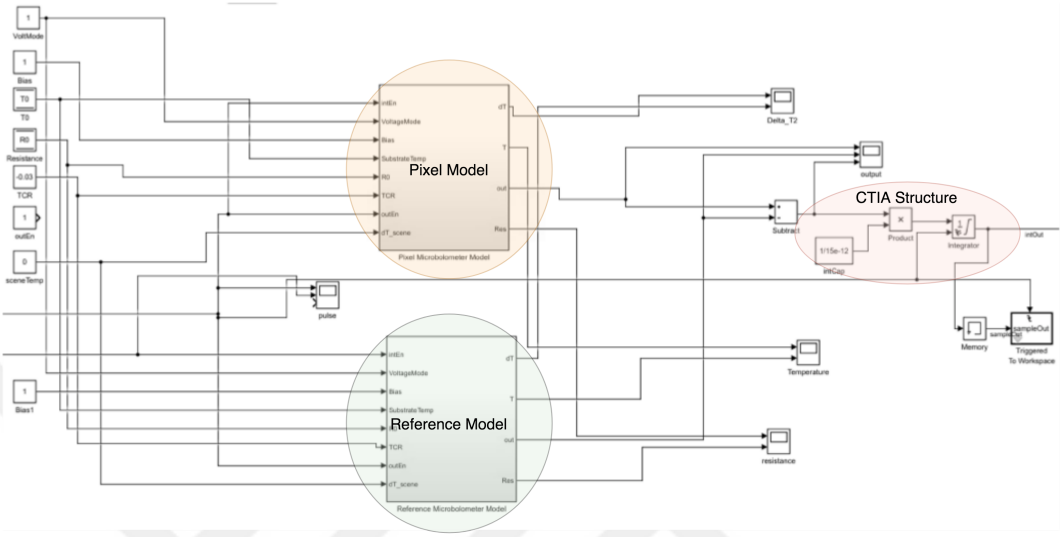

Figure 2.7 Simulink model CTIA integrator incorporating simulink model of Pixel and Reference Resistances

Figure 2.8 shows the Simulink model output for an active pixel and a reference resistance changes and integrator output voltage change during the integration time. The active pixel and reference resistor bias voltages are adjusted to keep the integrator output voltage at the equilibrium point for 300K substrate temperature. As can be seen from Figure 2.8 the integrator output voltage drops below the equilibrium point, after which it again starts to increase monotonically. It should be noted that the integrator output voltage might hit negative saturation for high gain applications resulting in reduced integration time and hence exacerbated performance.

The reference pixels are shared across the pixel array due to size limitations. This phenomenon dictates the reference pixels' thermal characters to be not exactly matched with the active pixels. Therefore, the reference resistance and active pixel resistance values are affected by the substrate temperature differently. As a result, integrator output voltage changes with the substrate temperature change, which is called as temperature drift. Figure 2.9 shows that the integrator output saturates when the substrate temperature changes by 10 K. The bias voltages must be calibrated for different substrate temperatures in classical readout to prevent output voltage

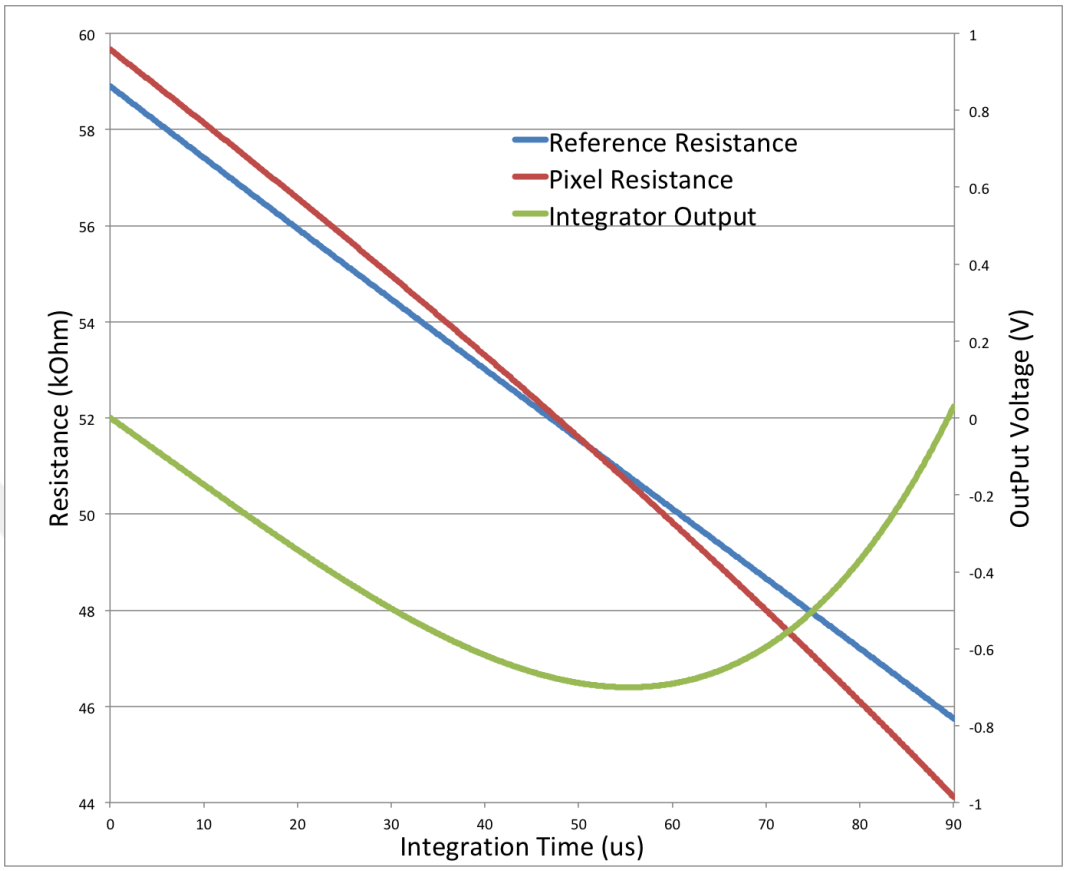

Figure 2.8 Pixel, reference resistance, and integrator output during integration time

saturation and to remove temperature drift.

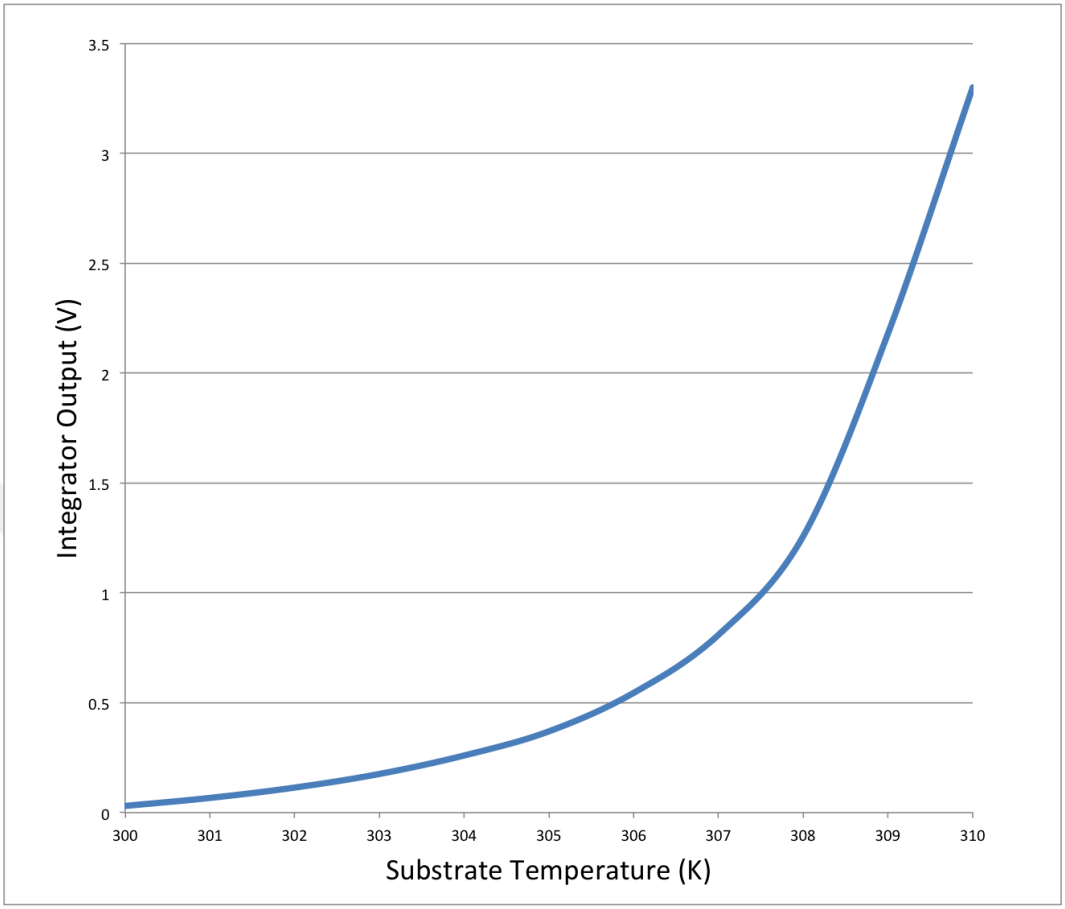

Figure 2.9 Integrator output voltage with respect to the substrate temperature

2.5 Conclusion of Chapter 2

This chapter summarized the performance metrics of the resistive type microbolometer sensors and calculated the minimum resolvable resistance change for a typical microbolometer resistor of a type YBaCuO or $V0_x$. This chapter also introduced the microbolometer imaging array and building blocks.

Chapter 2 continued by describing the self-heating effect and the elimination methods. The impact of self-heating on the active pixel and reference resistors and the output voltage is stated with the simulation results. Besides, this chapter introduced the voltage drift during the substrate temperature change.

In Chapter 3, VCO-Based Microbolometer Readout Architecture will be introduced and the design approach will be discussed. Section 4.7.2 will use the Simulink model to validate the proposed architecture in terms of performance and self-heating cancellation.

CHAPTER 3

BACKGROUND ON VCO BASED ADC

This chapter briefly summarizes the concept of VCO-based ADCs. The studies on the VCO-based ADCs mainly increase as the technology node shrinks. As the technology node shrinks below 65nm, the supply voltage level decreases, and hence the voltage headroom required to design an ADC decreases. The low supply voltage also results in a low dynamic range in the conventional ADC structures. Furthermore the transistor gain drops at the low technology nodes while the thermal noise components do not change. Therefore, at the advanced technology nodes signal to noise ratio of conventional ADC structures decreases and designing high-accuracy analog components for the traditional ADC architectures becomes difficult [29–31]. Besides, digital circuits occupy a minimal area at the advanced technology nodes, making it possible to design complex circuits with lower power dissipation. Because of aforementioned reasons, VCO-based ADCs became popular as they are highly digital structures with operation capability at low supply voltages [32].

The remainder of this chapter is organized as follows. Section 3.1 summarizes the VCO-based ADC architecture, and the properties of the architecture are given in Section 3.2. Section 3.3 discusses the quantization techniques of time-to-digital converters while the main drawbacks of VCO-based ADCs and the proposed solutions in the literature are reviewed in Section 3.4. Section 3.5 concludes this chapter.

3.1 VCO based ADC Architecture

Figure 3.1 shows the concept of time-domain ADCs. First, the analog voltage input is converted to a time-domain signal, then this time-domain signal is digitized. There

are various methods for converting an analog signal into a time-domain signal, and digitizing the time domain signal [33].

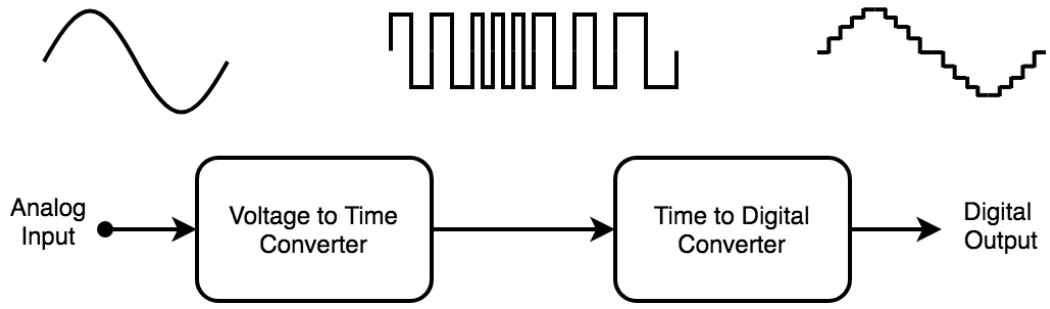

Figure 3.1 Concept of time domain ADCs

VCO-based ADCs use two-stage conversion. The ring oscillator used in the first stage integrates analog input signal and converts it to a frequency (or phase). The first stage is mostly implemented by using inverters or delay elements. As the technology nodes get finer, FO4 delays decrease significantly. A decrease in FO4 delays increases the resolution of the delay elements. In the second stage, the time-domain signal is transformed to a digital code proportional to the ring oscillator output frequency using either a digital counter or a phase sampler. VCO-based structures using the phase sampling approach [34–36] are mainly used to perform quantization function in sigma-delta ADCs. In addition to their use in sigma-delta ADC's, VCO-based structures are utilized as stand-alone ADC (open-loop) blocks in various applications [37–39]. In [37], VCO-based ADC with a digital counter in the second stage is used for on-chip noise measurement of a digital supply. Another VCO-based ADC design reported in [38] demonstrates 12-μV/LSB performance, which combines both digital counter and phase sampling approaches. The structure presented in [39] shows that VCO-based ADC's are also utilized as voltage-sensing readout circuits for various sensor applications. The main advantage of the design in [39] is claimed to eliminate the need for a pre-amplifier for better hardware efficiency.

3.2 VCO based ADC Properties

This section analyzes the VCO-based ADC stages and shows the advantages and disadvantages of this structure. First, this section explores the small signal of the

VCO stage. VCO output phase, $\phi[n]$, for a given sampling period can be written as

$$\phi[n] = \int_{(n-1)T_s}^{nT_s} 2\pi(K_{vco}v_{in}(t) + f_{fr})\,dt, \tag{3.1}$$

where T_s is the sampling period, n is the sample number, K_{vco} is the voltage to frequency gain of the oscillator, $v_{in}(t)$ is the analog input voltage, and f_{fr} is the free-running frequency of the oscillator. The sinusoidal input of $Acos(w_{in}(t)$ is applied as the input of the oscillator to analyze the frequency spectrum of the circuit. The output phase can be solved as

$$\phi[n] = A_\phi cos(\frac{w_{in}T_s}{2}(2n-1)) + f_{fr}T_s, \tag{3.2}$$

where A_ϕ is the gain factor due to the input signal. A_ϕ can be expressed as

$$A_\phi = 2\pi K_{vco}AT_s sinc(f_{in}T_s), \tag{3.3}$$

where f_{in} is the frequency of the input signal. As can be seen from the gain analysis, the input signal is low pass filtered with sinc function. This low pass filtering means that the oscillator filters out high-frequency noise component of the input signal. Equation **3.3** also states that the output phase change is directly related to the oscillator gain, K_{vco}. The direct relation between the output phase and the gain is the main disadvantage of this ADC structure since the linearity of voltage-controlled oscillators degrades at high input voltage differences.

Voltage controlled oscillator is implemented mostly using ring oscillators. Figure 3.2 shows three possible ways of implementing ring oscillators;

- **Supply Voltage Modulation**: The voltage supply defines the voltage swing of the inverting elements. The change in the supply causes the delay of the inverting stages to change, hence the oscillation frequency changes.
- **Supply Current Modulation**: The current of the inverting stages also defines the delay of the stages. The change in the supply current causes the delay of the inverting stages to change. Consequently, the oscillation frequency

changes.

- **Load Modulation**: Changing the load capacitance or resistance of the load causes the delay of the stage to change. The change in delay results in variation in the output frequency. This modulation type is mostly implemented using varactor-like structure, whose capacitance varies with the applied voltage.

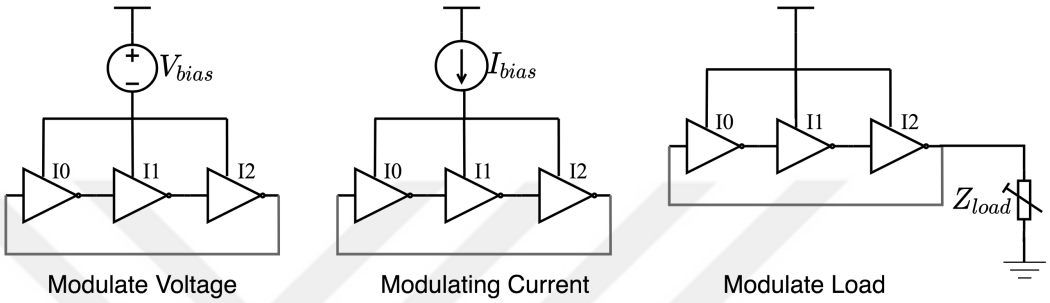

Figure 3.2 Ring oscillator implementation examples

3.3 Time to Digital Converters

Time to digital converter circuits convert the phase of the oscillator into the digital signal. There are mainly 3 ways to implement time to digital converter, i.e., quantizer. These are measuring the frequency of the oscillator and measuring the phase change of the oscillator, and combining frequency and phase measurement approaches. All of these methods require an external sampling signal as a reference point.

3.3.1 Frequency Measurement

Measuring the frequency can be thought of as measuring the period of VCO signals. Frequency measurement can be implemented by counting the VCO output clock within the predefined time interval. Figure 3.3 shows the counter-based VCO quantizer approach. As can be seen from the figure, the analog input changes the frequency of the oscillator. The reset counter counts the number of VCO output edges within the sampling clock period. During the sampling period, the counter takes the mean of the oscillator's frequency. This type of quantizer is mostly implemented for low-speed applications, where the oscillation frequency is much higher than the sampling frequency. As this work uses rolling line type of operation, the frequency

measurement approach is adopted in this thesis as the time to digital conversion. The sensitivity of the quantizer is limited by the sampling period, T_{win}, which is stated as

$$LSB = 1/T_{win}. \tag{3.4}$$

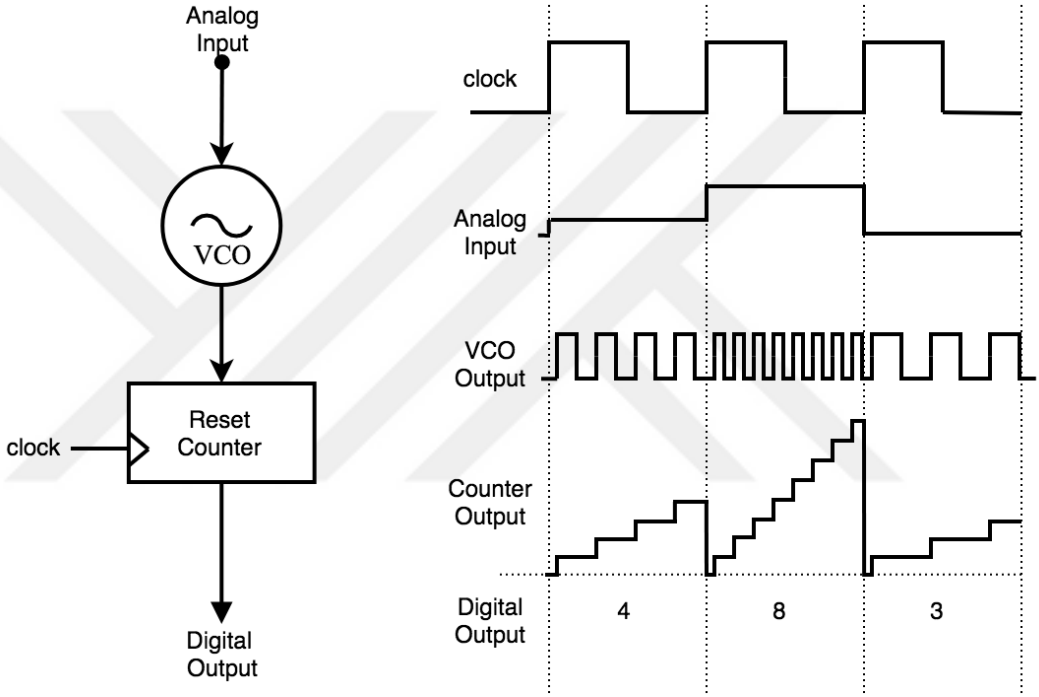

Figure 3.3 VCO based ADC with frequency measuring quantizer

The resolution of this approach can be increased in two ways. The first one is also to sample the negative edge of the oscillator output. In this way, the phase shift of 180 degrees can be differentiated. The second method requires implementing multiple counters for all phases of the oscillators. Implementing multiple counters also decreases the phase shift sampling resolution. The first method requires designing dual edge-triggered flip-flops. Both of these methods use higher power and a larger layout area to increase the resolution.

3.3.2 Phase Measurement

The phase measurement approach measures the change of VCO phases in a predetermined clock pulse. Figure 3.4 shows the example phase values for a 3-stage ring oscillator structure. As can be seen from the figure, only one phase changes in the oscillator structure to accomplish oscillation. This approach tries to record the phase change amount and relate it to the analog input signal. Therefore, the oscillator phase is sampled with a high-frequency clock with at least twice the oscillation frequency. This type of converter is mostly used when the VCO Based ADC is adopted in delta-sigma ADC structures. This approach is highly dependent on the oscillator clock output signal. Therefore, special care should be taken to decrease the jitter of the oscillators.

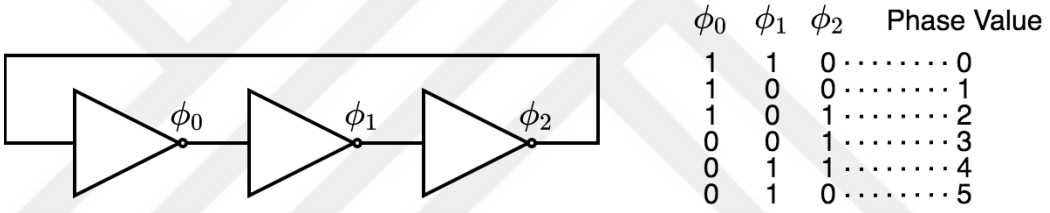

Figure 3.4 Phase Change diagram for 3 stage ring oscillator

Figure 3.5 shows the phase measurement quantizer. As can be seen from the figure, the sampling clock registers all of the phases and compares them with the previous ones to sense whether the phase changed or not. The total phase change amount is summed at the final stage of the structure to form an overall phase change. The sampling clock for this type of digitization circuit should be at least twice of the VCO frequency. Therefore, this type of quantization is used mostly in delta-sigma ADCs as an oversampling converter. As the reference clock frequency increases, the SNR of the ADC increases directly for this type of quantization approach.

The high-frequency clock samples the output of each phase of the oscillator and counts the phase change between the consecutive sample times. One phase change between the successive reference clock cycle means that the delay of the VCO cell is equal to the reference clock signal's period. The relation between the high-frequency

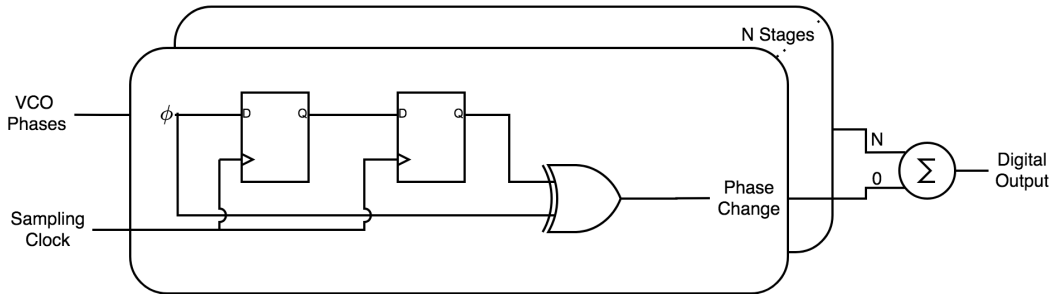

Figure 3.5 Phase measurement quantizer for N stage oscillator

clock frequency and the VCO delay can be given as

$$t_d = \frac{1}{Kf_s}, \tag{3.5}$$

where t_d is the VCO delay time, which is directly related to the analog input, K is the phase change amount, and f_s is the frequency of the sampling clock. VCO frequency, f_{VCO} with N inverter stages can be calculated as

$$f_{VCO} = \frac{Kf_s}{N}. \tag{3.6}$$

This relation means that the VCO frequency can have values with a step size of $\frac{1}{f_s}$. The phase output values of the quantizers are averaged in the desired time resolution of ADC to form a corresponding digital output. The $\Delta\Sigma$ ADC structure uses decimation filters at the output stage to increase the resolution and eliminate the out-of-band quantization noise.

3.3.3 Combining Frequency and Phase Measurement

The last method combines both to increase the sensitivity of the measurement at the expense of an increase in layout area and power. Figure 3.6 shows the block diagram of the combined approach in [38]. The counter starts counting the oscillator output positive edges, and records the oscillator phase info. At the successive positive edge of the sampling clock, the number of oscillator pulses is counted, and the phase change between the successive samplings is calculated. These two outputs are combined to form a finer resolution output.

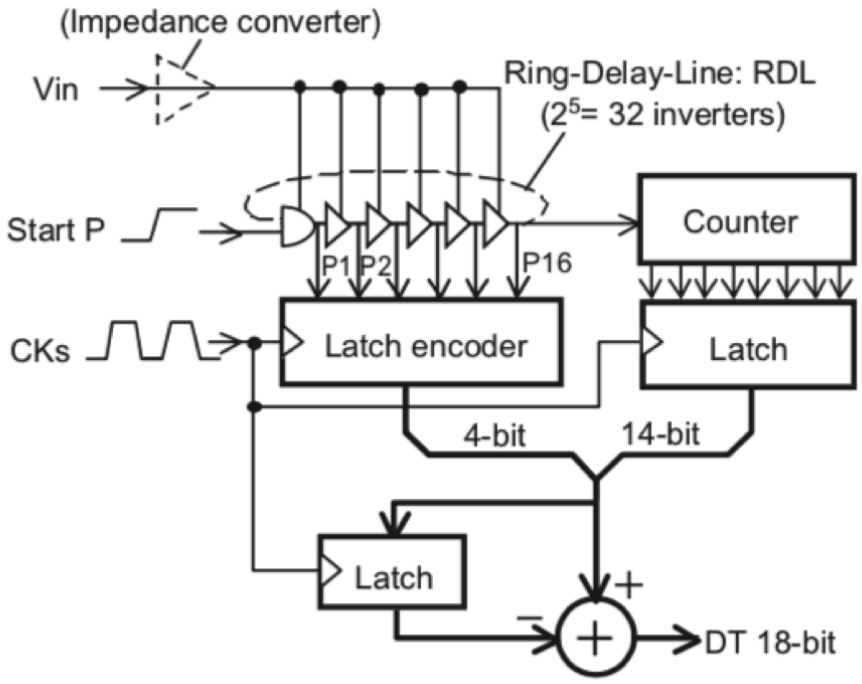

Figure 3.6 Combining frequency and phase measurement [38]

3.4 VCO Nonlinearity

Oscillators are mostly implemented using back-to-back inverters for the VCO-based ADCs. The oscillation frequency is highly dependent on the gain of the oscillator, as stated in Equation **3.3**. Figure 3.7 shows an example curve of VCO output frequency with respect to the input voltage. As can be seen from the figure, VCO gains decrease with the excess increase or decrease of input voltage. This non-linearity is the main drawback of the VCO-based ADCs.

The use of VCO structure as an ADC is minimal due to the nonlinear behavior of the oscillator. Highly nonlinear tuning characteristics introduce severe harmonic distortions in voltage to frequency conversion, and it limits the ENOB to 6-7 bits [40]. There have been several techniques to improve linearity in VCO-based quantizers [35, 41–48]. These correction methods can be grouped into 2 main categories; minimizing the signal swing of the oscillator input voltage, and implementing calibration algorithms.

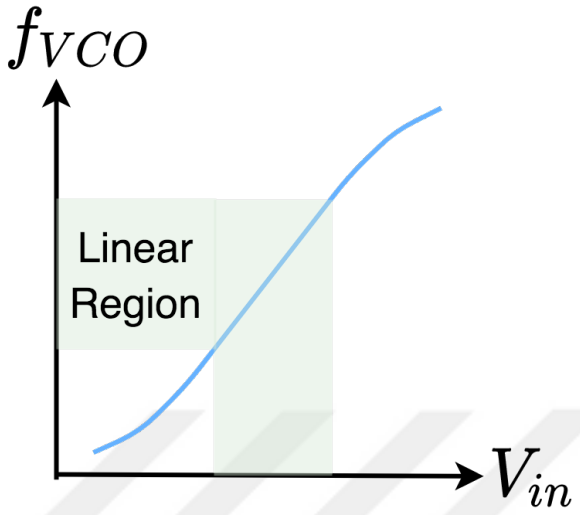

Figure 3.7 VCO frequency vs voltage input curve

Minimizing the input swing is realized by using the VCO-based quantizers inside $\Delta\Sigma$ loop [42, 45]; $\Delta\Sigma$ loop is designed to force the oscillator in desired input voltage swing, i.e., in the linear tuning curve region. Another technique is using a PWM modulated signal as the input voltage. PWM modulated signaling also forces the oscillator to create well-defined outputs [47]. As seen from the referenced articles, most of these quantizers are used as the quantizer for $\Delta\Sigma$ architectures.

There are also calibration algorithms for open-loop architectures. These algorithms can be categorized as foreground and background calibration algorithms. Although the foreground calibration technique is easy to implement, it does not provide real-time adaptation to temperature changes or other process flows. Therefore, mostly background calibration techniques are implemented [49]. There are various kinds of background calibration techniques, split ADC structures [50], replica VCO structures [43], lookup table-based calibration algorithms [49]. These background calibration techniques mainly try to linearize the nonlinear tuning curve using extra analog circuits and digital logic.

3.5 Conclusion of Chapter 3

This chapter summarized the concept of VCO-based ADCs by examining the structure in terms of sub-blocks and signaling and stated the works in the literature about the VCO-based ADC structures. This chapter described the various methods for designing a ring oscillator for analog to time-domain signal conversion. Time to digital conversion methods is also introduced and examined with the example wave diagrams.

The realization of the VCO-based ADCs becomes with the advancement in CMOS technology with a finer resolution process. As technology nodes shrink, the voltage headroom decreases, and the need for mostly digital ADC architecture increases. As a result of this need, the literature about this architecture increased rapidly within the last ten years. Besides, at the low feature size process nodes, the inverter FO4 delay significantly decreases. The analog signal processing capabilities decrease for the low feature size process nodes due to reduced gain and voltage headroom.

Similarly, the same almost digital design approach can also be adopted in microbolometer readout circuits to achieve reduced space and lower power consumption. In this work, benefiting from the VCO-based approach, a novel microbolometer readout architecture utilizing a VCO-based ADC with a digital counter in its second stage is implemented. The proposed method can potentially achieve the goal of reducing area and power dissipation for microbolometer readouts.

CHAPTER 4

VCO BASED MICROBOLOMETER READOUT ARCHITECTURE

In this chapter, the proposed architecture for microbolometer readout circuits is introduced. The VCO-based architecture enables a low power and low area microbolometer readout circuit. The prototype test circuit includes the analog signal chain of the readout circuit. The building blocks of the proposed microbolometer readout architecture are reviewed and the simulation results and the circuit parameters are reported. This chapter also introduces two readout techniques for self-heating calibration.

The test circuit is designed and fabricated at TSMC 65nm CMOS Low Power Process node and manufactured through Europractice multi-project wafer (MPW) design service. However, detecting materials could not be grown on top of the test circuit since test IC is not produced as a full wafer. Therefore, the test circuit could not be used as a stand-alone imager.

This chapter is organized as follows. Section 4.1 introduces test circuit architecture, and Section 4.2 gives the pixel array implementation. Then Section 4.3 analyzes the VCO Based Column Readout circuit. The bias generator block, the digital controller block and the top level integration of the test circuit are discussed in Section 4.4, Section 4.5, and Section 4.6 respectively. Section 4.7 explains the proposed self-heating calibration algorithm. Finally, Section 4.8 finalizes this chapter.

4.1 Test Circuit Architecture

The novel microbolometer readout circuit includes the analog signal chain, the programming interface, and bias generators. Figure 4.1 shows the block diagram of test circuit. Test circuit mimics the imaging array in a small form factor to take the array effects into account when calculating the imaging performance. Test IC includes a 4×4 pixel array, a 1×4 reference pixel array, a 1×2 column readout, a digital controller, a bias generator, and a parallel to the serial output driver circuit. Test circuit also has the capability of connecting external off-chip resistances for both pixel and reference.

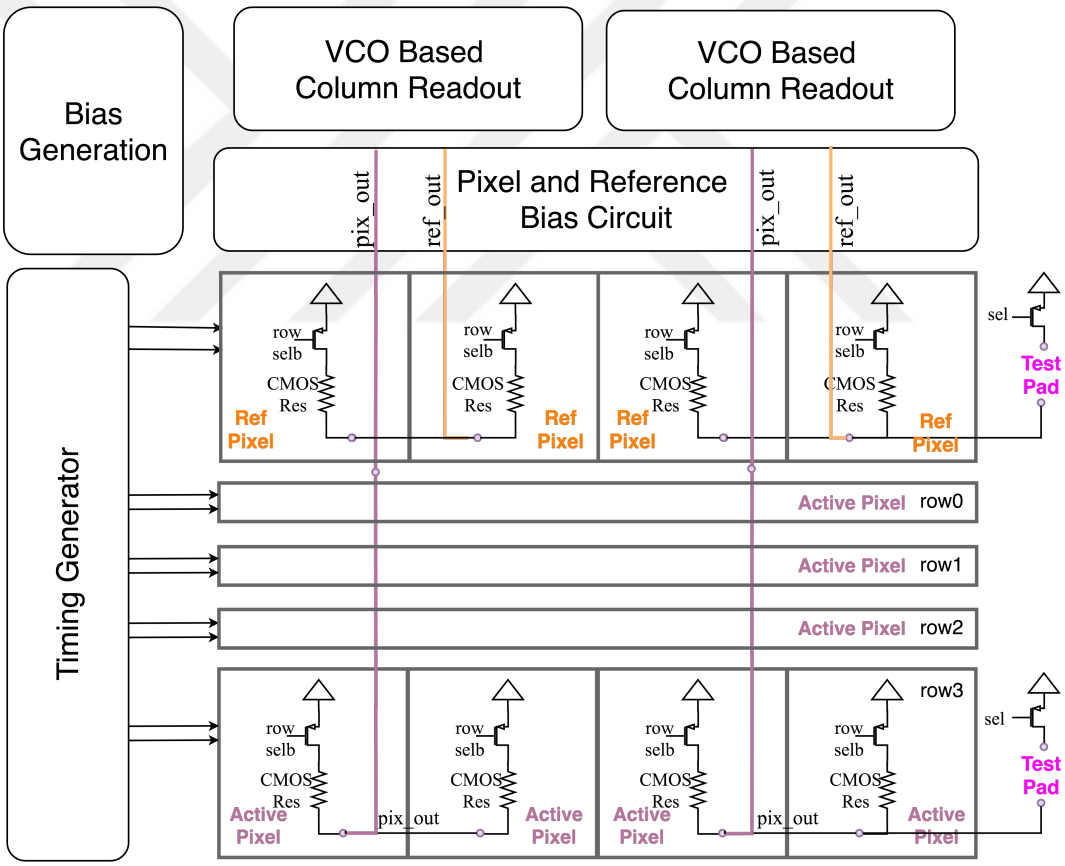

Figure 4.1 Test circuit top level block diagram

Figure 4.2 shows the analog signal chain of the readout architecture, which determines performance of the microbolometer readout circuit.

The analog signal chain of the readout architecture, given in Figure 4.2 determines the performance of the microbolometer readout circuit. In this approach, the pixel resistors are biased with constant current sources, and the voltage across them is measured, unlike the classical method, implementing voltage bias and current measurement. In the proposed design, the voltages across the resistances are measured. The difference between the active pixel voltage and reference (blind) pixel voltage is then used in the column readout circuit for amplification. Taking the difference eliminates bias heating-related voltage change of the active microbolometer pixel and common-mode noise components due to bias current and supply voltage. The column readout circuit first converts the voltage difference into two current signals using a transconductance amplifier. These current signals are then amplified, integrated, and digitized by two current-controlled oscillators. The digital output of these oscillators is subtracted, and the final digital value is obtained. The following sections will discuss the implementation details and the performance parameters.

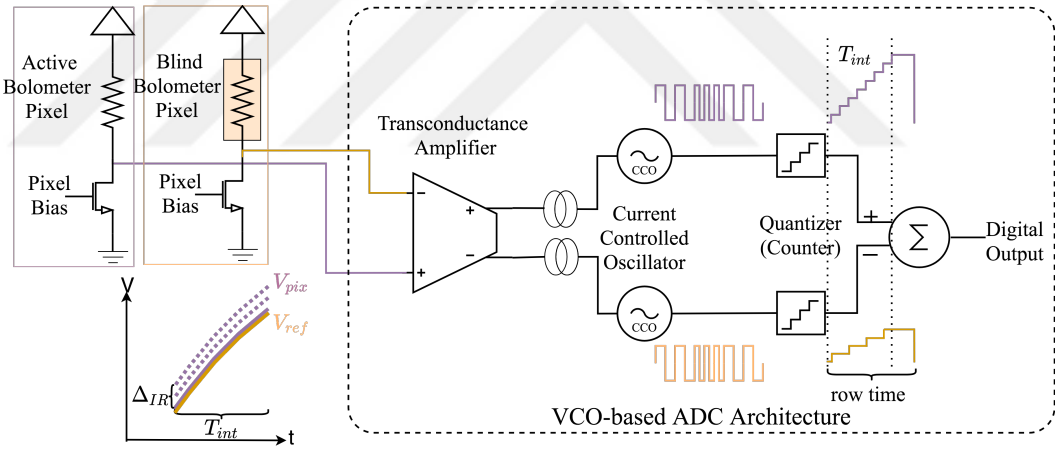

Figure 4.2 Proposed readout architecture

4.2 Pixel Array

Pixel circuit creates voltage output for both pixel and reference resistances for a constant bias current. Pixel Array includes 4×4 active pixel circuit, 1×4 reference pixel circuit, pixel bias circuits, pixel row scanner, and connections to the input/output pads for microbolometer tests. Each pixel in the array has 60kΩ CMOS resistance and selection switch. Figure 4.3 shows a block diagram of the pixel array structure

for test IC. As can also be seen from the figure, the neighboring pixels are treated as another row since the column pitch is twice the pixel pitch. Therefore, the digital controller and the pixel circuit are arranged to drive eight rows. Pixel and reference bias circuit copies the current created at the bias generator to active and reference pixels, respectively. The digital controller can program the following features of the pixel array:

- Connecting the CMOS test resistances at active and reference pixels
- Connecting the Active and reference pixels to output pads
- Selecting the number of rows
- Activating the active and reference biases

Figure 4.4 shows the single-pixel circuit; with resistors and transistors' noise models included. The readout architecture uses the voltage difference between the active and reference pixel nodes, as in Figure 4.2. The noise of the pixel bias voltage is common for both active and reference pixels and hence can be eliminated. Total voltage noise at the pixel output node is calculated as

$$v_{n,pix}^2 = R_{pix}^2\left(\frac{8kTg_{m,M0}}{3} + g_{m,M0}^2\frac{K_n}{C_{ox}W_{M0}L_{M0}}\frac{1}{f}\right) + 4kTR_{pix} * \gamma, \qquad \textbf{(4.1)}$$

where R_{pix} is the nominal pixel resistance value, k is the Boltzmann constant, T is temperature, g_m is the admittance value of transistor, f is the frequency, terms with K, W and L is the gain, width, and length of transistor respectively, C_{ox} is the oxide capacitance of transistor, and γ is the flicker noise correction factor of bolometer resistance.

The voltage noise at the output of reference resistance can be calculated with the same method. These two noise sources are not correlated and will be treated as equal in the following stages for simplicity. Therefore, overall voltage noise will be calculated as two times the value of Equation **4.1**. In this equation, The flicker noise components of resistors depend on the detector materials and not easy to determine. Therefore, the flicker noise component of a resistor is assumed to be γ times the thermal noise component of a resistor. The bias transistors, M0 and M1, are kept as

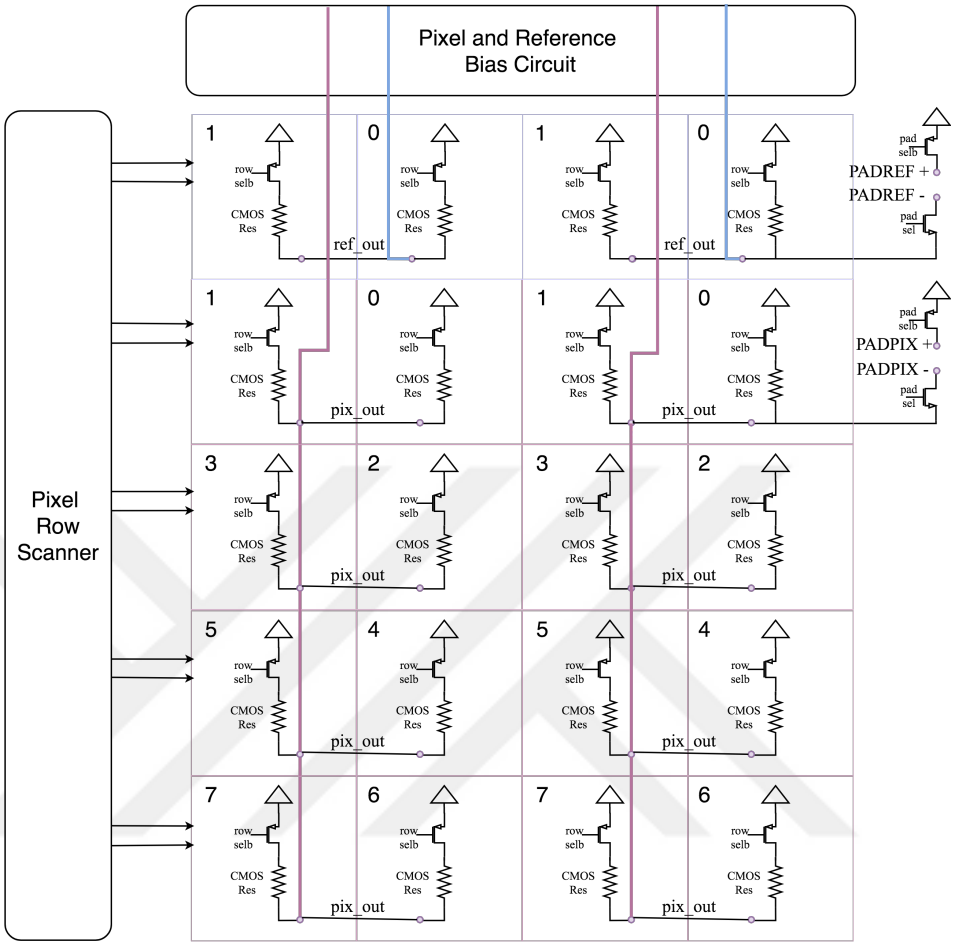

Figure 4.3 Test IC pixel array structure

large as possible to decrease the output noise. Therefore, they are not placed in each pixel and placed right below the column readout.

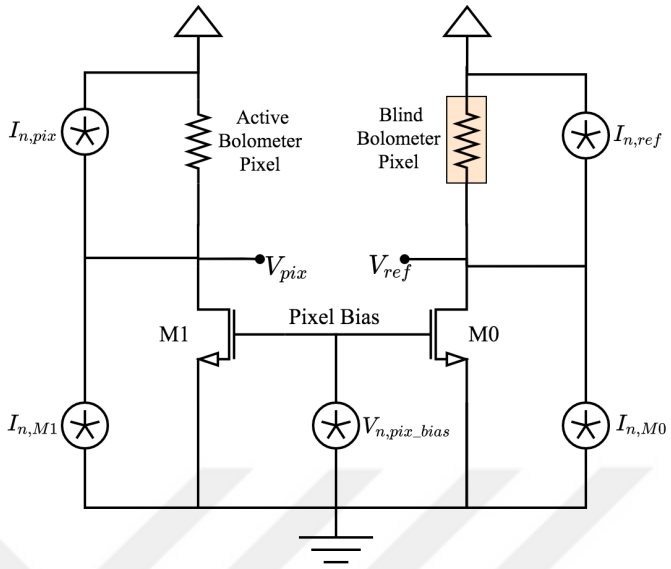

Figure 4.4 Pixel circuit with noise sources

4.3 VCO-Based Column Readout

The column readout circuit converts the difference of pixel and reference resistance voltage outputs to a digital value. The column readout circuit implemented in this thesis uses a pseudo-differential VCO-based approach. Figure 4.2 shows the block diagram of the column readout circuit, named as VCO-based ADC architecture. As seen in this figure, the column readout architecture comprises three parts: transconductance amplifier, current-controlled oscillator, and quantizer (time-to-digital converter). Transconductance amplifier converts the voltage difference between active and reference pixels into currents. These two currents are used at the current-controlled oscillator and quantizer circuits to form a digital value. At the final stage, the difference of the digital values are subtracted to create an output value. Figure 4.5 shows the layout view of the column readout circuit, which occupies 50 μm by 110 μm area.

4.3.1 Transconductance Amplifier

A differential Operational Transconductance Amplifier (OTA) is used to convert the difference of pixel and reference resistance voltages to a differential current. Figure 4.6 shows the schematics and transistor dimensions of the transconductance

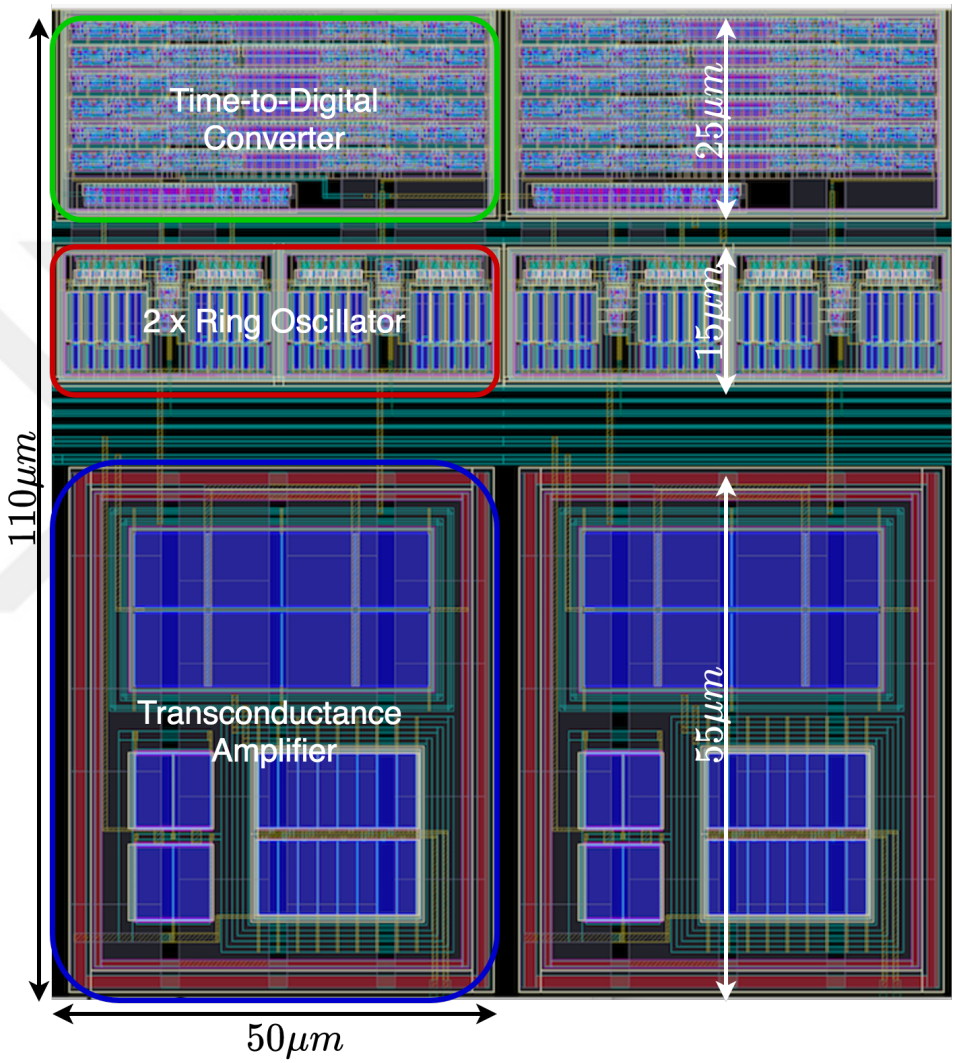

Figure 4.5 Layout of 1×2 column readout

amplifier. Unlike other parts of the column readout circuit, which work with 0.9 V supply, transconductance amplifier supply voltage is set to 1.2 V. This voltage level is required for getting the required voltage headroom at the pixel bias circuit. This part is the only analog block.

Bias	Value
ibias_p	9.2 uA
ibias_n	5.8 uA
I_out (dc)	1.2 uA
supply	0.9 V

Device	W/L
M0, M5, M6	32u/8u
M1, M2	32u/4u
M3, M4	64u/2u

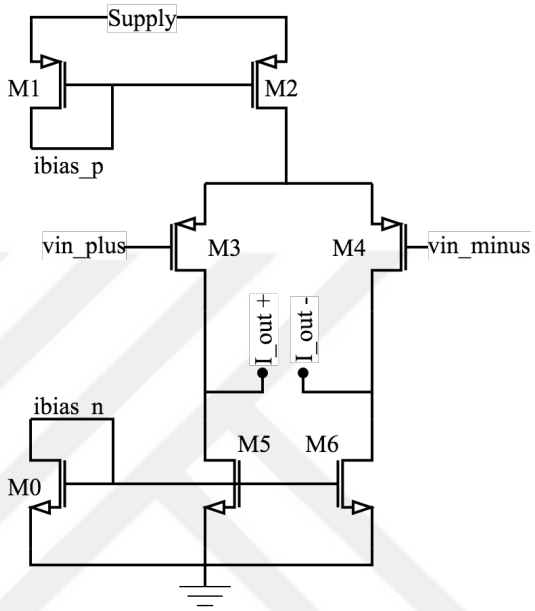

Figure 4.6 Schematic of transconductance amplifier

This OTA employs two constant current sources (ibias_p and ibias_n) and current mirror transistors; M2, M5, and M6. The difference between these current sources defines the base current at the output nodes. The base current of the output nodes is set to 1.2 μA at the initial configuration. However, the magnitude of the current sources can be modified through a programming interface to change the center frequency of oscillation. The difference of input voltages is converted into current using differential input transistors; M3 and M4. These transistors define the small-signal gain of this amplifier and is set to $100\mu A/V$ at default configuration.

The transconductance amplifier and the pixel bias circuit are at the input front-end of the column readout circuit; the noise component of the transconductance amplifier is directly added to the pixel noise components. The noise component of the pixel circuit is investigated in Equation **4.1**, and the input-referred noise of the

transconductance amplifier can be calculated as follows

$$v_{n,in}^2 = \underbrace{8kT\frac{2}{3g_{m,M3}} + \frac{2K_p}{C_{ox}W_{M3}L_{M3}f}}_{noise\ due\ to\ M3,\ M4} + \underbrace{8kT\frac{2g_{m,M5}}{3g_{m,M3}^2} + \frac{2K_n}{C_{ox}W_{M5}L_{M5}f}\frac{g_{m,M5}^2}{g_{m,M3}^2}}_{noise\ due\ to\ M5,\ M6}, \tag{4.2}$$

where terms with g_m are the admittance value of transistors, f is the frequency, terms with K, W, and L are the gain, width, and length of transistor respectively, C_{ox} is the oxide capacitance of the transistor. The transconductance amplifier's output noise is directly related to the g_m of M3, and M4, which is set to be $100\mu A/V$. Another factor affecting the noise performance is the flicker noise of the mirror transistors; M5 and M6. The dimensions of M5 and M6 are kept as high as possible to decrease the flicker noise components.

4.3.2 Current-Controlled Oscillator

The current-controlled oscillator structure converts the output current of the transconductance amplifier into a time-domain signal. Time-domain conversion is carried out by back-to-back connected inverters. Figure 4.7 shows the schematics of the 3-stage and 5-stage oscillators with selection switch and rail-to-rail buffers. The output current of the transconductance amplifier is directed towards either 3-stage or 5-stage oscillator structures via a selection switch. The same selection signal also selects the output of the rail-to-rail buffers to create a time-domain signal output. When one of the oscillator structure is selected, the other oscillator structure is forced to remain in a quiet state by driving the start signal statically.

Figure 4.8 shows the schematics of a 5-stage ring oscillator architecture. The oscillator circuit is mainly composed of inverters and start logic. Although it is not given in this figure, rail-to-rail converters are connected to phase outputs of the inverting stages. Start logic is activated (logic low) when the integration starts and becomes inactive (logic high) after the digitization. Therefore, no residue comes between the consecutive read operations.

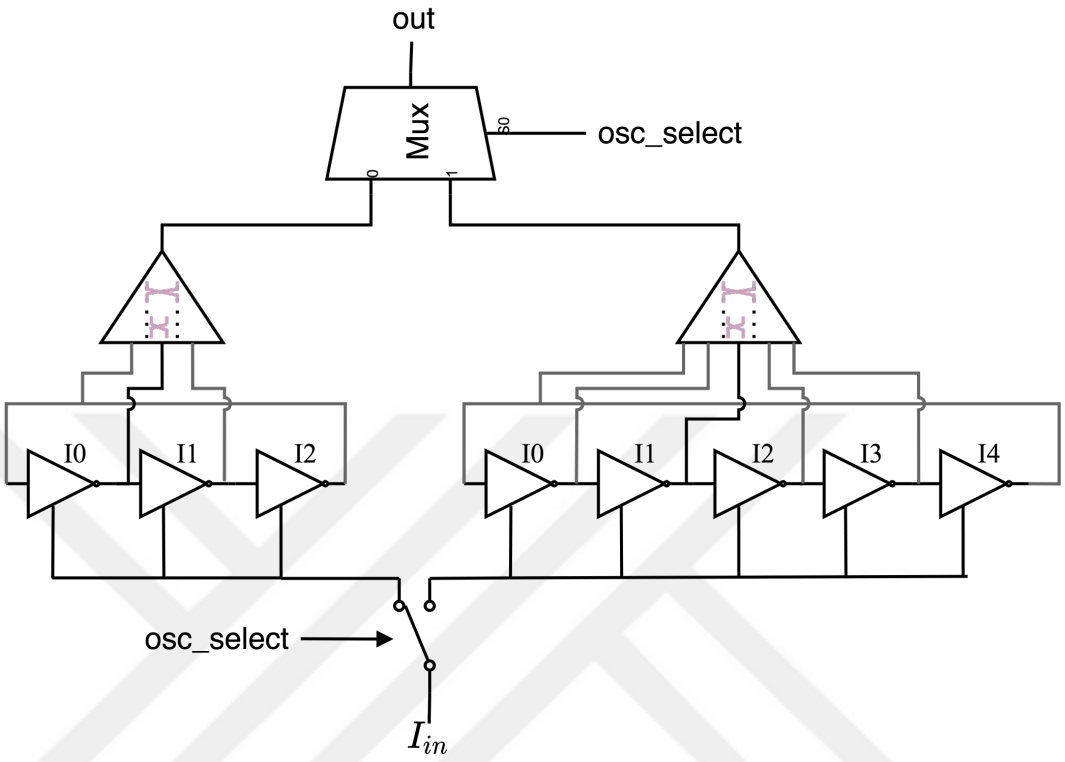

Figure 4.7 Two ring oscillator structure

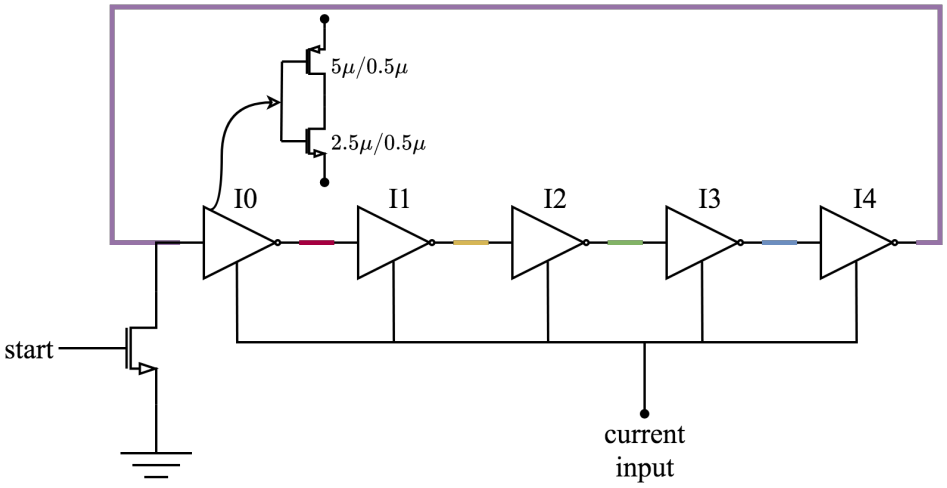

Figure 4.8 Schematic of 5-stage ring oscillator

Ring oscillators need to satisfy Barkhausen's criteria to oscillate, as stated in [51]. This condition states that the overall phase shift should be equal to 180 degrees with an overall gain bigger than 1. The small-signal gain of each inverter stage can be calculated as

$$H(jw) = -\frac{g_m R_o}{1 + jw_0 R_o C_l}, \tag{4.3}$$

$$\theta(jw) = tan^{-1}(w_0 R_o C_l), \tag{4.4}$$

where H is frequency-dependent gain, g_m is total admittance of NMOS and PMOS transistors, R_o is the parallel output resistance of transistors, C_l is the load capacitance of an inverter, and w_0 is the frequency of interest. 5-stage ring oscillator needs 36 degrees of phase shift, i.e., θ, at each stage for an oscillation. This yields

$$w_0 R_o C_l = tan(36) = 7.7. \tag{4.5}$$

However, [51] also states that the oscillation frequency and w_0 defined in the above equations might not necessarily be the same. These criteria are needed for the oscillation to start. For a ring oscillator, the oscillation frequency is defined by the delay times at each stage. Each inverter in the ring oscillator drives the gate capacitance of proceeding stages and rail-to-rail buffers. Figure 4.9 shows the example output waveform for a 5-stage ring oscillator when the start logic is activated. This figure shows that inverter output voltages oscillate between 400mV and 900mV voltage levels, and only one inverter supplies current through its PMOS transistor to the transconductance amplifier. The inverter output low-to-high transitions, and hence rise time is defined by PMOS transistors. However, high-to-low transition, hence fall-time, of the inverter outputs are constrained by the residue current defined at the transconductance amplifier. As can be seen from the figure, the period of output wave is composed of 5 falling delays, determined by the input current. Therefore, the oscillation period is defined by the number of inverting stages, N, multiplied by the delay of each inverter, t_d.

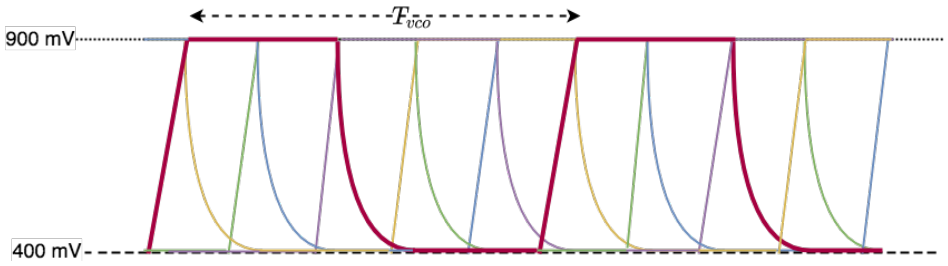

Figure 4.9 Example output wave diagram of 5-stage ring oscillator structure

The delay time, t_d, of each inverter stage is calculated as

$$t_d = \frac{C_l V_{sw}}{I_{bias}}, \tag{4.6}$$

where V_{sw} is the switching voltage headroom of the inverter, and I_{bias} is the current bias of the inverter. This yields a frequency of oscillation, f_0, and current-to-frequency gain, K_{cco}, of the oscillator for N inverter stage as

$$f_0 = \frac{1}{N t_d}, \tag{4.7}$$

$$K_{cco} = \frac{1}{N C_l V_{sw}}. \tag{4.8}$$

Test IC implements two ring oscillator structures, 3-stage and 5-stage ring oscillators, respectively. The selection signal controls the current flow and the start signal of the oscillator structure. When one oscillator is selected, the other structure remains in a known state and dissipates no power. As can be seen from Figure 4.5, the oscillator structure occupies 15 $\mu m \times$ 50 μm area, which is very small when compared with the capacitance-based integration scheme used in the classical readout architecture. The layout area could further be decreased when one of the oscillators is selected at the imaging applications. Reducing the layout area makes it possible for the integration of the column readout circuit under the pixel array layout.

Figure 4.10 shows the simulation results of oscillators' frequency with respect to

input current carried out at with a transient analysis sweep using Cadence Spectre tools. The oscillators' low voltage is kept constant at 400 mV voltage levels, and the input current is changed from -500 nA to +500 nA with a step size of 10 nA. At each step, one phase of the oscillators' period is measured, and the oscillators' frequencies are calculated. Although in the real application, the low voltage of the oscillator could not be kept constant, this simulation shows the approximate gain level of the current-controlled oscillator structures. The 3-stage ring oscillator structure has a higher center-frequency and higher gain ratio than the 5-stage ring oscillator at the expense of dynamic range. The gain of 3-stage and 5-stage ring oscillators are obtained as 14.2 THz/A, 8.2 THz/A, respectively, at Spectre simulations. From these gain results, the load capacitance for each stage can be calculated as 46 fF. This load capacitance includes gate capacitance of both the next stage and the output buffer.

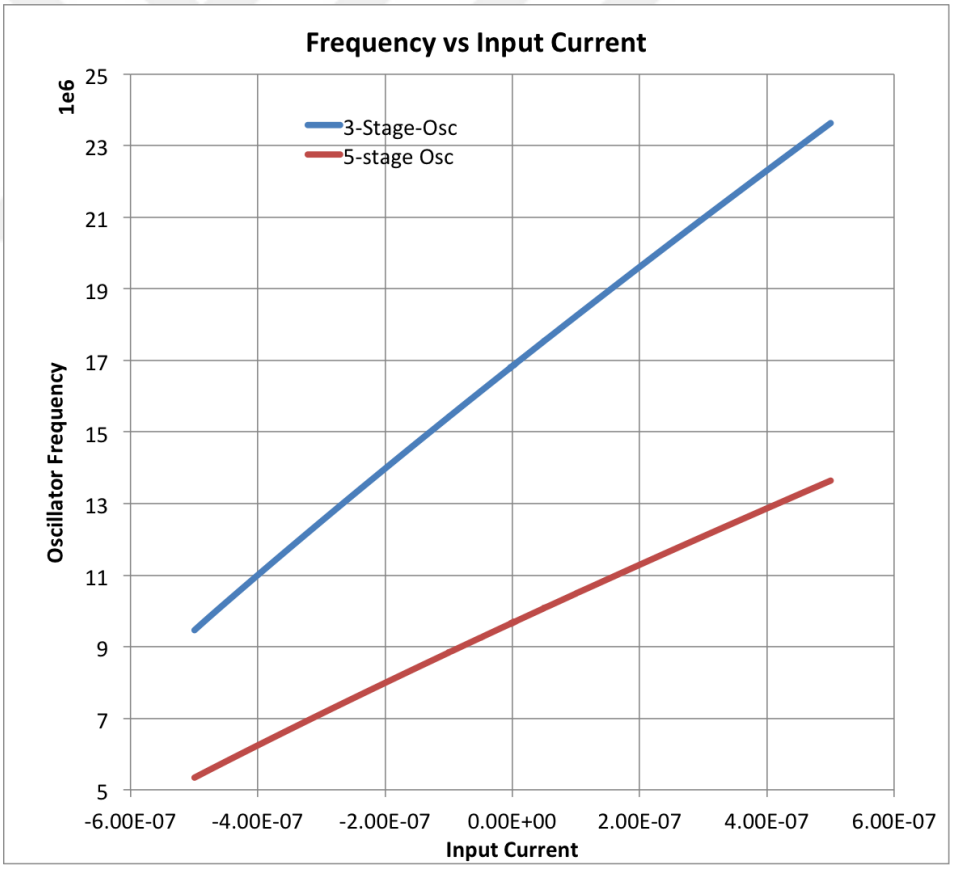

Figure 4.10 CCO frequency vs input current for 5-stage and 3-stage configurations

4.3.3 Time-to-Digital Converter

Both the plus and minus oscillator outputs need digitization to convert the resistance difference into a digital signal. Figure 4.11 shows the block diagram of this digitization, which is implemented using an asynchronous counter. The counter-based digitization approach implements a 12-bit toggle counter, which includes six 2-bit counters connected serially. The digital signal of the oscillator output drives the LSB of the structure, which increments with. This counting scheme is very similar to a clock divider circuit, and the power dissipation is minimal since only one flip-flop is driven with a high-frequency oscillator clock. The counters are reset to a known value before the integration starts with the signal named as *count_resetb*, this causes the VCO-based ADC to digitize from a known initial state, together with the *start* signal of oscillators. The digital output, i.e., the counter value of plus and minus oscillators, is subtracted from each other to form an image-related digital output value, which is 13-bit long. This digital output is later sampled by the parallel in serial out (PISO) driver circuit.

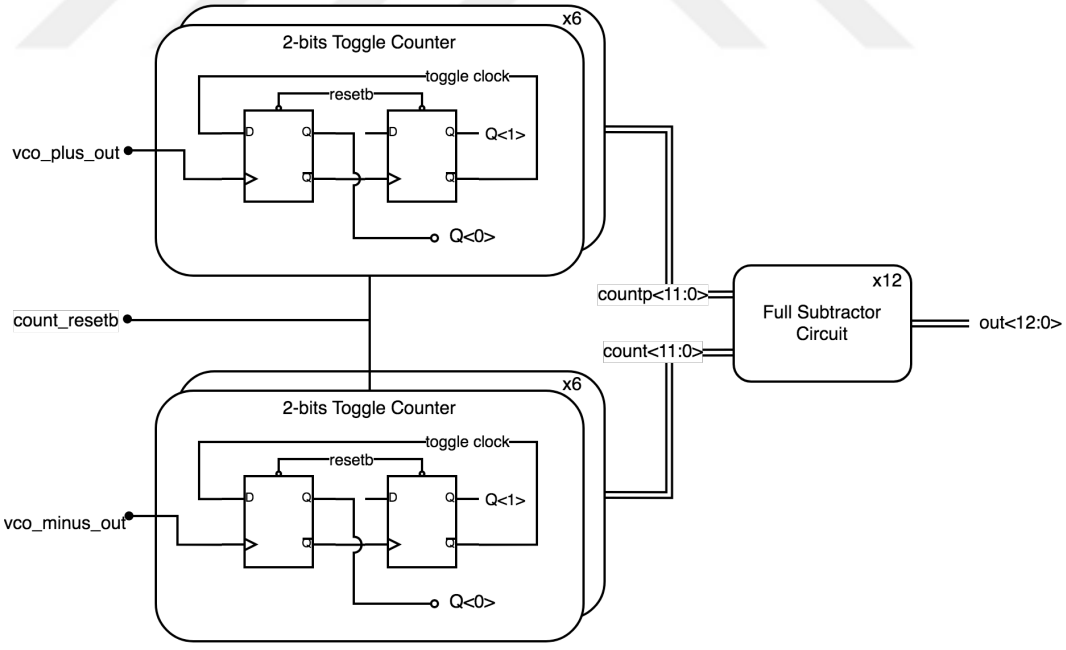

Figure 4.11 VCO output to digital output creation circuit

Toggle counter simply averages the frequency of VCOs for a time window of counting, T_{win}.

$$LSB = 1/T_{win} \tag{4.9}$$

states that the sensitivity of the counter circuit increases as the sampling window increases, requiring a higher integration time. The increase in the integration time results in the decrease of 2 important performance parameters: frame rate and dynamic range. The integration time increase increases in the row time and frame time, and hence decreases the frame rate. When the integration time increases, the counter circuits count for a longer time and can quickly saturate with the lowest change in the input circuit due to high gain. The quick saturation results in a lower dynamic range compared with the lower integration time.

The overall gain of readout chain with respect to input resistance can be found as

$$LSB = \frac{2NC_lV_{sw}}{g_{m-diff}I_{bias}T_{win}}, \tag{4.10}$$

where T_{win} is the integration window, I_{bias} is the bias current of pixel bias, g_{m-diff} is the differential gain of transconductance amplifier, V_{sw} is the voltage swing of oscillator outputs, C_l is the load capacitance of inverters of the oscillator, and N is the number of inverter stages at the oscillator. This equation shows that the gain increases as the load capacitance of the inverting stage increases. Therefore, this readout technique must be implemented in low feature size process nodes with smaller capacitance values.

Each column readout circuit drives a 13-bit signal as the output. To decrease the pad number, parallel outputs are serialized using a simple shift register circuit with a parallel inputs load feature. Shift registers are loaded with a 13-bit signal when the *load* signal is activated. Figure 4.12 shows the digital signals controlling the readout circuit. As can be seen from this signaling scheme, after the selection of row, first the counters are reset with *count_resetb* signal, then the VCO's are activated with *start* signal. When the integration time ends, first the VCO's are de-activated, then the output of subtractors are sampled with *load*.

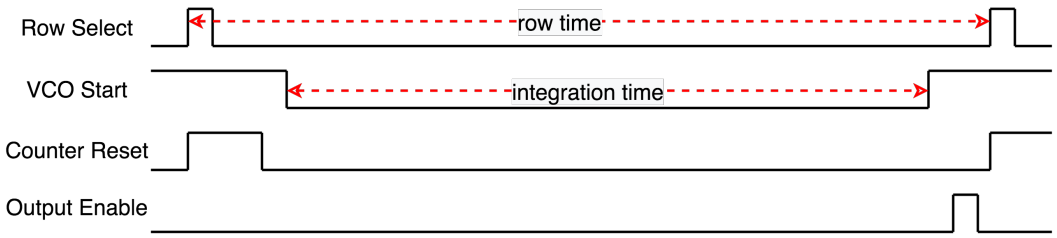

Figure 4.12 VCO based column readout digital control signals

Transient noise simulations with Cadence Spectre environment are carried out to verify the performance of the proposed architecture before manufacturing. Transient simulations include the response of column readout to the differential input voltage. Figure 4.13 shows the simulation results of column readout of 3-stage oscillator structure with respect to a differential input voltage sweeping from -1 mV to +1 mV. This figure also plots the change of plus and minus output frequencies during the sweep. The voltage to frequency gain is obtained as 677 MHz/V and 396 MHz/V for 3-stage and 5-stage oscillator structures. The digital output gains are also calculated as 1.2×10^5 Counts/V and 0.7×10^5 Counts/V for 3-stage and 5-stage structures.

The noise performance of the structure is also simulated with Cadence Spectre Tool. Transient noise analysis is carried out with 50 samples, and the digital output of the structure is recorded. Figure 4.14 shows the digital output histogram obtained from this transient noise analysis. The standard deviation of the obtained outputs are calculated as 2. This means that the structure has 2 LSB counts noise for an integration time of 100 μs.

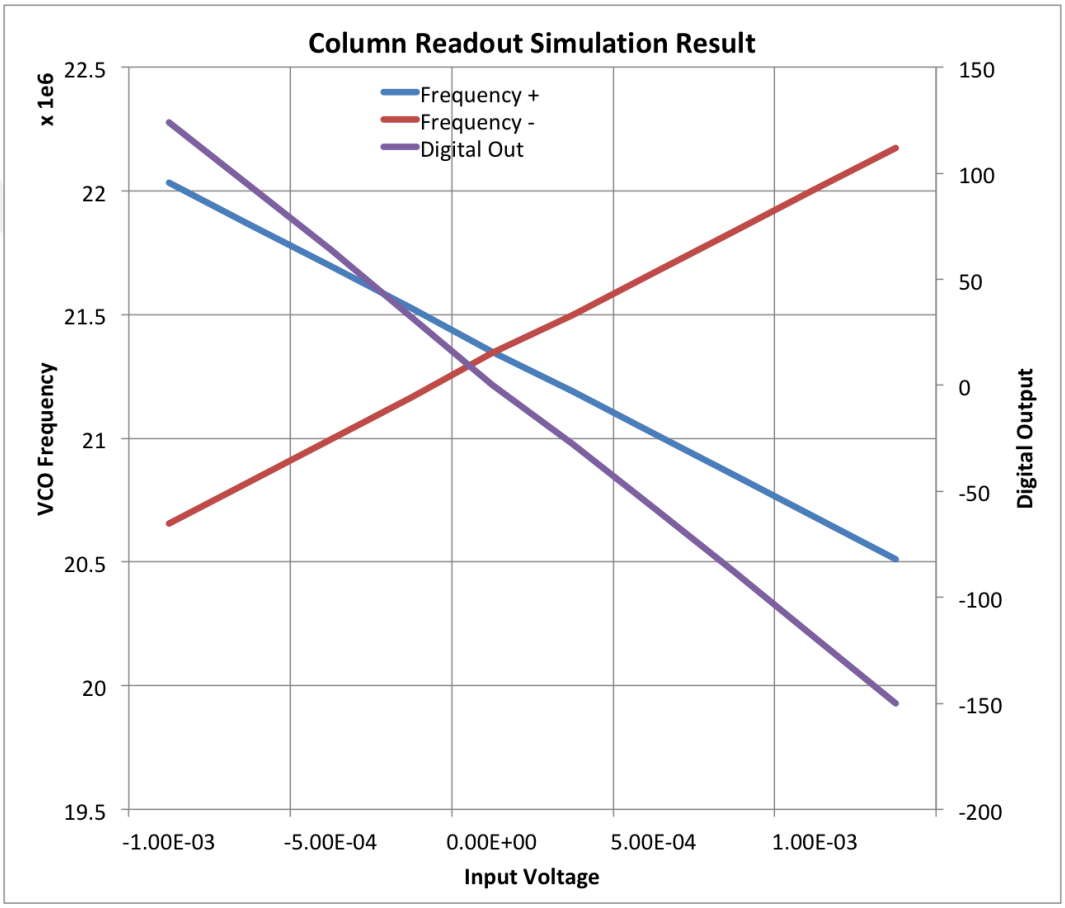

Figure 4.13 Column readout simulation results with respect to differential input voltage

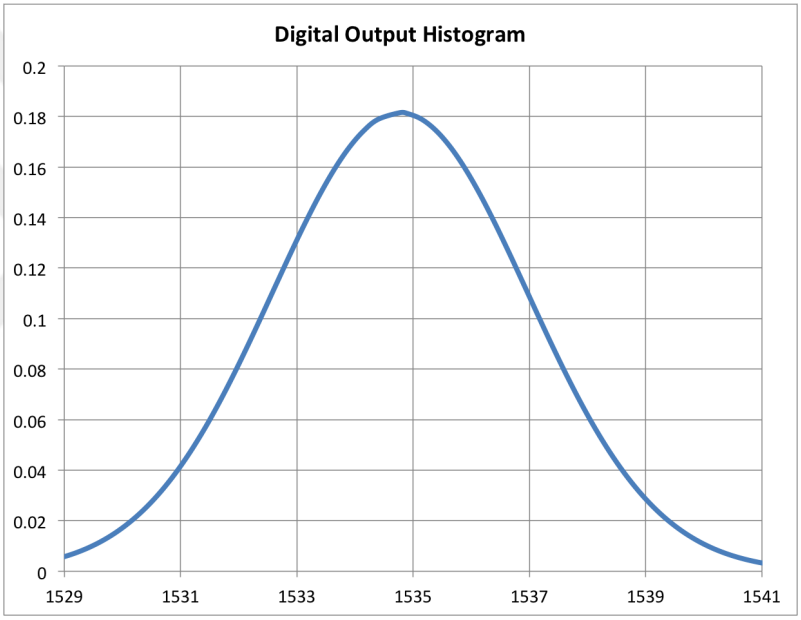

Figure 4.14 Digital output histogram obtained from transient noise analysis

4.4 Bias Generator

Bias generator creates the required bias currents via on-chip programmable current sources. Test IC requires six current sources; four current sources for pixel array, one for pixel bias, one for reference bias, two for testing, and two current sources for the transconductance amplifier. 9-bit programmable current mirror circuit is designed to create these current sources from the master current source. These current mirrors multiply the master current according to the control switches, which activates the current multiplying transistors. These switches are designed to be programable through the memory block of the digital controller, which can be programmed via the digital programming interface of the chip. Supply independent master current is created by using Widlar type of current reference, shown in Figure 4.15. This circuit works with 1.2 V analog supply voltage and arranged to produce 10 μA master current. 2 test points: *vpbias* and one of the master current ($I_{out} < 0 >$), are also connected to the output pad for debug purposes.

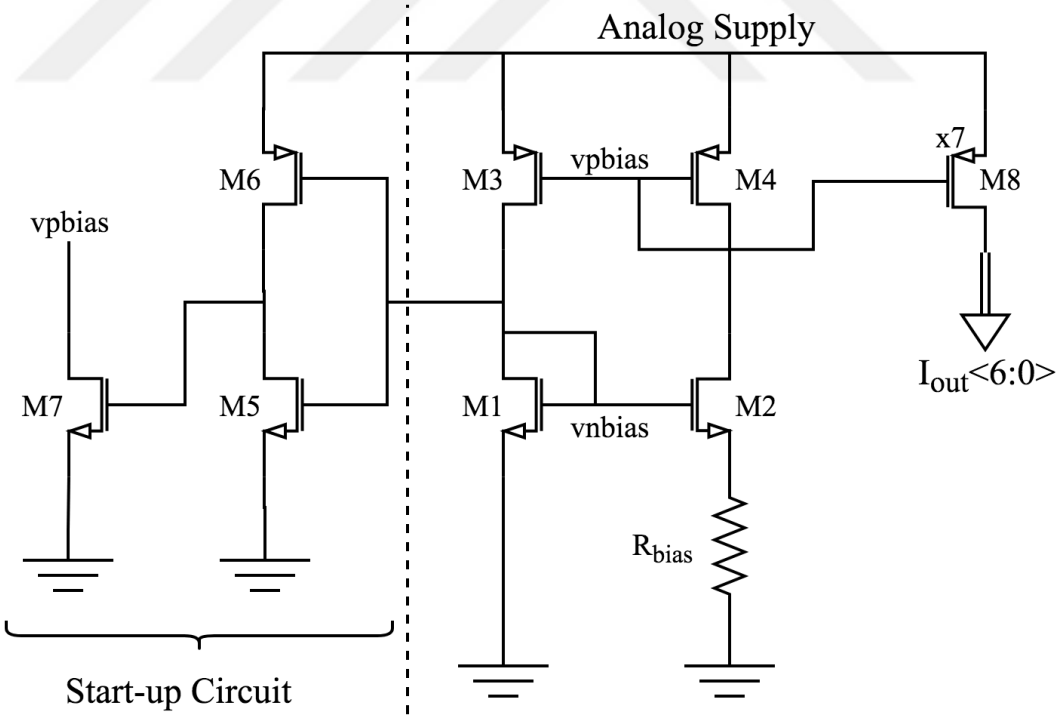

Figure 4.15 Schematics of widlar type master current generation

Widlar type master current generation includes two parts; main circuit and start-up

circuit. Main circuit includes back-to-back connected two current mirrors; M3-M4 and M1-M2 transistor pairs; with an R_{bias} resistor connected to the source. M3 transistor mirrors the current flowing through M4 with a gain factor related to their parameters, and M2 transistor mirrors the current flowing through M1 with a gain factor related to their parameter ratios. The negative feedback between these two current roads makes this circuit stable at two points. When the current equations are solved, the master current flowing through M4 transistor can be extracted as

$$\sqrt{I_{out}} = \frac{1}{2R_{bias}} \left(-\frac{1}{\sqrt{\beta_2}} \pm \sqrt{\frac{1}{\sqrt{\beta_2}} + 4R_{bias}\sqrt{\frac{I_{out}}{\beta_1}}} \right), \tag{4.11}$$

where β_1 is the gain factor of M1, β_2 is the gain factor of M2. As can be seen from the equation, this equation yields two solutions; one is for zero current flow, and the other one is a real-valued current value. For the case of zero current flow, the voltage at *vpbias* node gets equal to the supply voltage. Therefore; start-up circuit is created to disturb this node other than the supply voltage. Start-up circuit simply reads the *vnbias* node voltage and upsets the *vpbias* node to take a value other than the supply voltage. By this way, *vpbias* node could not reside in at supply voltage levels. Therefore; this circuit yields a master current at the calculated value. Transistors M8 in the schematics mirror the master current to programmable current mirrors. Seven master currents are generated; six for the proposed architecture and one for testing the bias generator.

4.5 Digital Circuits

Digital Circuits are responsible for creating the signals of the readout circuit (given in Figure 4.12), programming the operating modes, and setting the bias currents of the readout circuit. The digital controller design consists of three parts to carry out these goals;

- **Programming Interface** enables the communication between the IC and out-of-chip components.

- **Memory Array** holds the value of the programmable sections of the IC.
- **Frame and Row Counters** keep track of the row time and frame time according to the row number and frame time values.
- **Signal Generation Blocks** generate the readout signals according to the row time signal.

Serial programming interface uses 3 signals; *clock*, *shift_en*, *shift_data*, to configure the internal registers of test IC. Figure 4.16 shows the schematics of the programming interface. This programming interface consists of two shift registers; shadow registers and programming registers. The external data in *shift_in* is shifted with a *clock* signal while *shift_en* is asserted. Sixteen bits of data are shifted towards the shadow registers. At the falling edge of the *shift_enable* signal, the shadow register values are passed to the main programming registers. Main programming registers directly control the memory array with the following bit sequence from MSB to LSB; 1-bit for write enable, 4-bits for memory address selection, and 11-bits for the memory data. When the write enable signal is active, the selected memory address is programmed with the 11-bit of data.

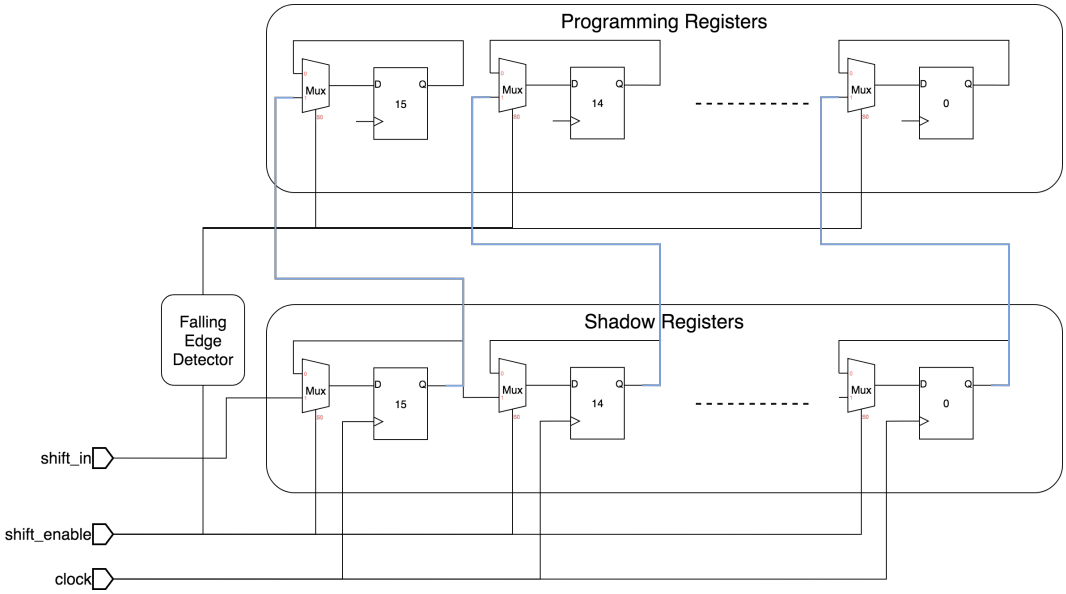

Figure 4.16 Schematics of serial programming interface

The memory array consists of 15 rows of 11-bit wide D-type flip-flops. Each flip-flop is arranged to hold its value unless the new data is loaded. Besides, flip-flops are programmed to have a reset value so that the test circuit can work without waiting to program all rows of the memory array. The programming register controls the write interface of the memory. MSB bit of the programming interface enables writing to the selected row of memory with the programmed data. 6 rows of the memory array holds the programming value of the current mirrors, 6 rows controls the timing signals, and 3 rows control the configuration and test outputs.

The microbolometer readout circuits generally work in a rolling line manner, and this means that the rows should be selected one by one, and this sequence should repeat itself every frame. The digital controller includes two counters; one is 10-bit, and the other one is 6-bit, to accomplish this goal. The first counter holds the row time, meaning the maximum number of this counter defines the row time of the readout. The readout signals are described with respect to the first counter to repeat at each row selection. The second counter increments with the output of the first counter and defines the frame time. The output of the second counter selects the rows consecutively. The memory array defines the maximum number of both counters for flexibility.

The last mission of the digital controller is to produce the readout signals. The column readout signals, given in Figure 4.12, are produced by the signal generation block. Figure 4.17 shows the signal generation block schematic including 10-bit counter. The signal generation block creates the pulse comparing the counter value with the signal start and signal stop values. When the counter value reaches the signal start value, signal out is asserted until the counter value reaches the signal stop value. Besides, the signal info pin can change the polarity of the output and force the output to the desired value. In this way, each of the three signals can be programmed very flexibly so that the IC's testability is increased.

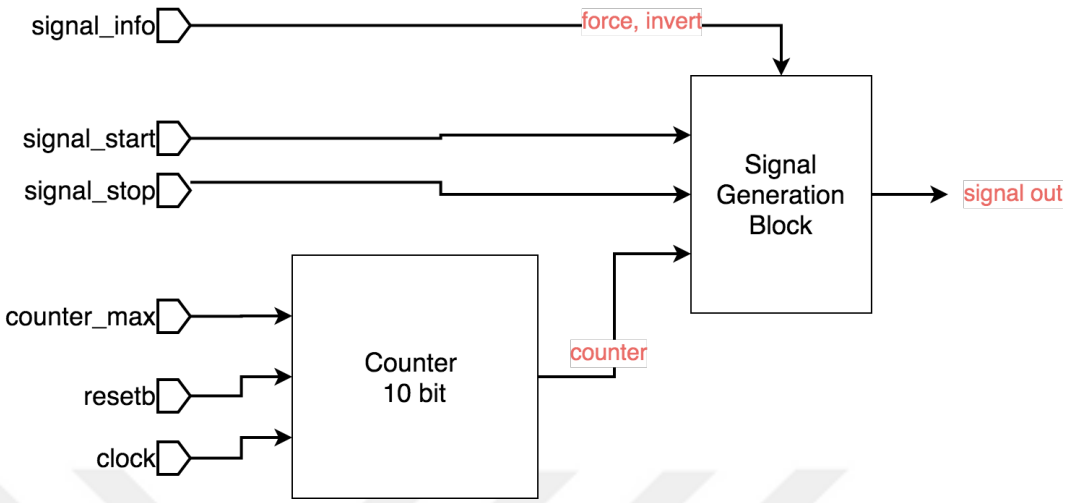

Figure 4.17 Block diagram of signal generation circuit with row time counter

4.6 Top Level Integration

The test circuit includes all of the above-mentioned sub-blocks. Test IC requires 20 pad connections for testing the functionality and debugging. Table 4.1 shows the pins and functions of Test IC. Pin list includes 4 digital input pads, 4 digital output pads, 6 analog IO pads, and 6 power pads. The digital circuit of the prototype works with 0.9 V voltage levels, whereas the digital IOs operate at 1.2 V voltage levels. Internal inverting mode level-shifters are integrated between the digital output of the chips and pads. Digital test output pin *digtest* can be configured to output internal test signals, however, its default value shows the output of serial programming connection. Besides, 4 analog pads are directly connected to the active and reference pixels, and 2 analog pads are connected to the bias generator circuit.

Table 4.1 Test circuit pin lists and functions

#	Name	Type	Voltage	Function
1	shift_en	IN	1.2 V	Serial programming interface data enable input
2	shift_in	IN	1.2 V	Serial programming interface programming data

3	clock	IN	1.2 V	Test IC clock signal, typically @ 1MHz
4	resetb	IN	1.2 V	Test IC active low reset signal, resets the memory
5	digtest	OUT	1.2 V	Test IC digital test output
6	dvdd	IO	0.9 V	Test IC digital power rail
7	dvss	IO	0	Test IC digital power rail
8	dvdd_io	IO	1.2 V	Test IC IO and ESD power rail
9	sub_gnd	IO	0	Test IC IO and ESD power rail
10	vnbias	IO	0.6 V	Widlar current generator, bias node voltage
11	itest	OUT	-	Widlar current generator, current test output
12	avdd	IO	1.2 V	Test IC analog power rail
13	avss	IO	0	Test IC analog power rail
14	out<0>	OUT	1.2 V	Test IC digital output of channel 0
15	out_valid	OUT	1.2 V	Test IC valid signal of digital outputs
16	out<1>	OUT	1.2 V	Test IC digital output of channel 1
17	pix_plus	IO	-	Active pixel pad connection
18	pix_minus	IO	-	Active pixel pad connection
19	ref_plus	IO	-	Reference pixel pad connection
20	ref_minus	IO	-	Reference pixel pad connection

Test circuit layouts are custom designed using Cadence design tools with the process design kits of TSMC 65 nm process node. Figure 4.18 shows the top-level layout of the test circuit. This test circuit occupies 400 $\mu m\times$ 400 μm layout area. As seen from the layout, the power ring structure incorporating analog and digital supply and ground signals surrounds the readout circuit. Test circuit core area occupies almost one-third of the total layout area. The digital controller occupies the biggest layout area in the core since it includes the memory array, and it is designed to be very flexible.

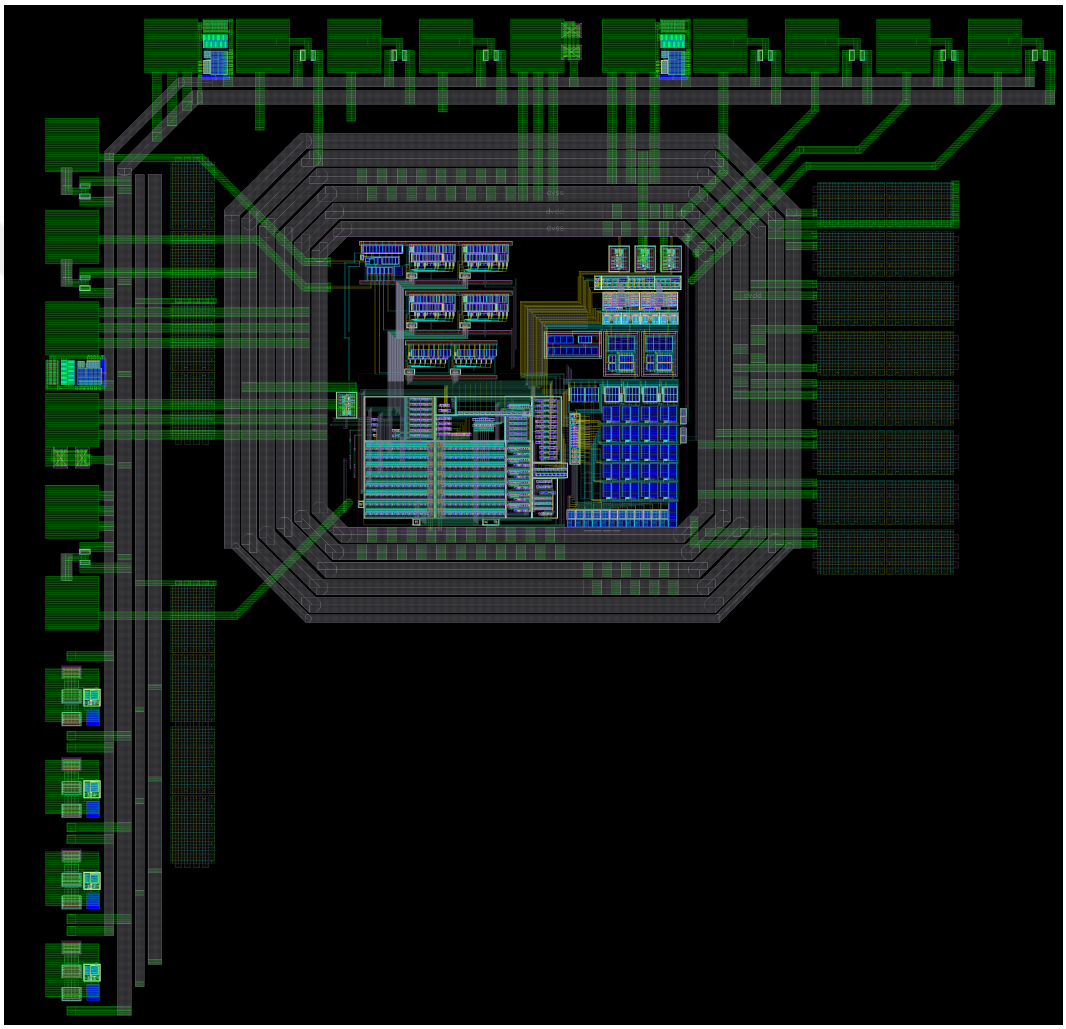

Figure 4.18 Test circuit top level layout

4.7 Self-Heating Calibration Method

One of the most critical factors affecting the microbolometer imager's performance is the ability to correct the self-heating effects. The classical microbolometer readout updates the self-heating impact by implementing column-level reference resistances, as mentioned in Section 2.4. This method states that the infrared blind microbolometer resistance is used to cancel out the offset removal for the active pixels. Section 2.4 also shows that the substrate temperature drift occurs since the thermal parameters of the active and reference pixels could not precisely be matched due to size limitations. VCO-based microbolometer readout architecture enables two methods for self-heating calibration:

- Infrared blind microbolometer reference resistances are used as in the classical readout approach.
- Finely adjustable CMOS resistances are used as the reference.

Using infrared-blind resistance approach is similar to the classical readout approach. The classical microbolometer readout implements the active and reference pixels in serial connections, such that the current difference is amplified at the CTIA amplifier, requiring a high voltage supply. However, VCO-based ADC amplifies the voltage difference between the current-biased active and reference pixels. Besides, the proposed approach uses the current bias approach as opposed to the classical readout.

VCO-based readout approach enables to use of CMOS resistor as the reference resistances. This method can eliminate the substrate temperature drift effect due to inexact matching of the thermal parameters of active and reference pixels. In this method, the CMOS resistances are changed by two different methods; open-loop control, closed-loop control. Both of these methods are implemented at test IC, and the memory bank controls selection. Both of these methods use 50 kΩ base resistance and 11 $\times$ 900 Ω serial resistance. Each node of the small resistances is connected to pixel bias voltage with a switch. These switches are controlled by a shift-register-based structure, forcing only 1-bit to be selected at a time.

4.7.1 Open-loop Control of CMOS Resistance

Open-loop control of CMOS resistance tries to mimic the change of the active microbolometer resistance. The CMOS resistance value is adjusted by fixed steps. Figure 4.19 shows the block diagram of the open-loop CMOS resistance control and the output waveform of the both pixel and reference resistance voltages. As can be seen from this figure, reference resistance decreases with fixed steps. This method tries to keep the voltage difference in a known range.

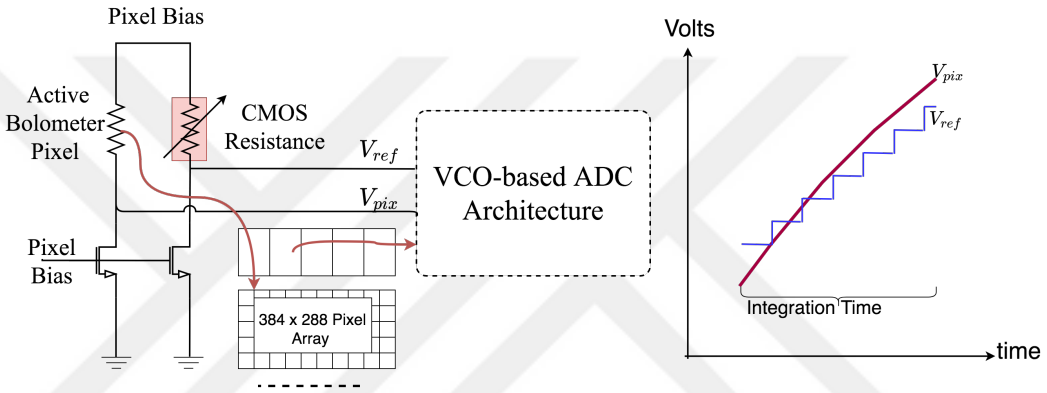

Figure 4.19 Open-loop control of CMOS resistance for self-heating calibration

The open-loop control of CMOS resistance approach requires that CMOS resistor be implemented at the column level. The initial value of CMOS resistance should be calibrated for each pixel since the nominal resistance of the pixels could not be exactly matched due to process variations. This type of calibration is similar to classical readout implementation, requiring bias adjustment for calibration of non-uniformity between pixel and reference resistances. CMOS resistance selection shift register sets the initial value and decreases the CMOS resistance at each time step. The microbolometer readout circuit implements a time step of 10 μs, controllable through a serial programming interface.

4.7.2 Closed-loop Control of CMOS Resistance

The closed-loop control of the CMOS resistance method consists of two channels; calibration and offset reduction channel, and readout channel. Unlike the open-loop control of the CMOS resistance method, this method requires implementing infrared-blind microbolometer reference resistors. The calibration channel includes the reference resistance. Calibration and offset reduction channel, named as $col0$ in Figure 4.20, compares the output voltage of current-biased row-based blind microbolometer resistance and CMOS resistances and tries to decrease the voltage difference by changing the CMOS resistance value through a resistor bank. Calibration algorithm checks for the plus and minus output of the counters at regular predetermined update instants and either increases or decreases the CMOS resistance value, as in Figure 4.21. This method limits the difference between the differential inputs of the transconductance amplifier and enables both VCOs to operate at desired linear current-to-frequency gain range. The calibration channel also sets for the initial bias current of the pixel value in substrate temperature changes.

In this architecture, to make the thermal and resistive parameters of the blind pixels match, a unique blind resistance is used for every active row. As seen in Figure 4.20, the calibration channel output is subtracted from the main channel output to form an infrared image. In this way, variations due to non-infrared effects such as self-heating and offset caused by substrate temperature variations are eliminated. Unlike the open-loop approach, this method uses blind microbolometer pixels but results in lower voltage differences at the readout channel. Lower input voltage yields better linearity at the oscillators.

To validate the effectiveness of the proposed bias heating calibration methods before tape-out, simulation flow, given in Figure 4.22, is created. A Matlab Simulink model is developed as in [28]. The Simulink model uses thermal component parameters and extracts resistance values during the integration time for constant current bias. The resistance obtained from Simulink is used as the microbolometer resistance in Cadence Spectre simulations, and the digital output of the readout channel is recorded for different offset resistances. CMOS resistance selection algorithms are arranged to work ten times during the integration time of 100μs, typical integration

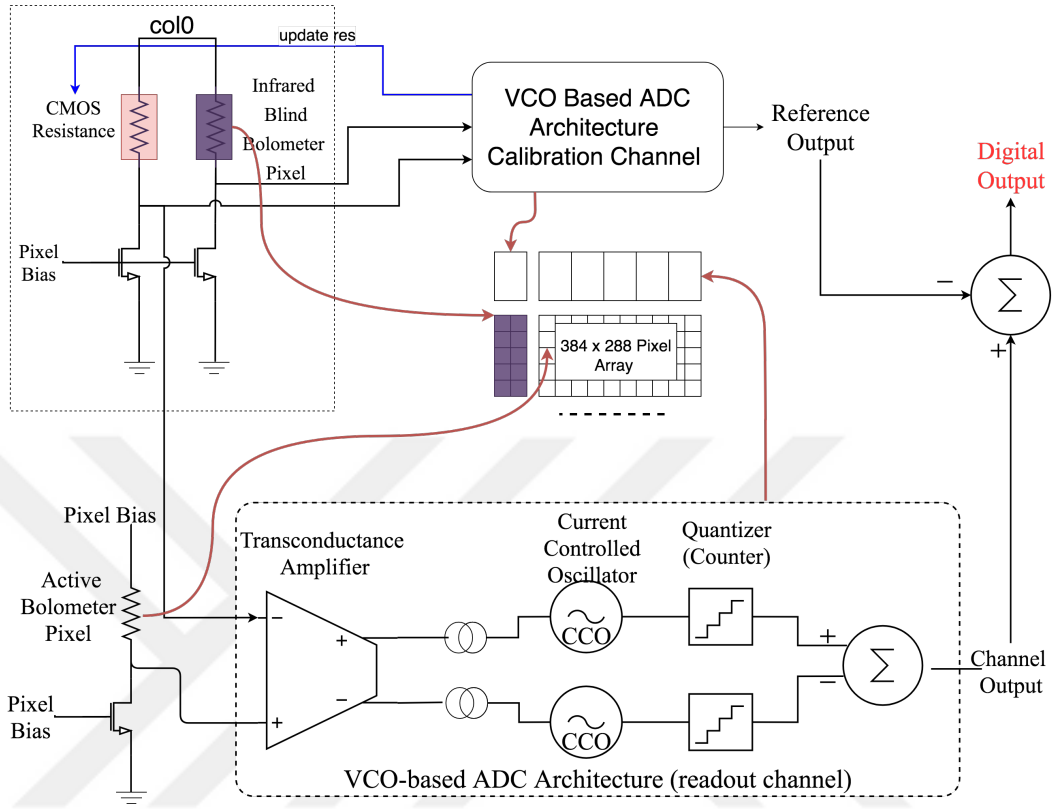

Figure 4.20 Closed-loop control of CMOS resistance for self-heating calibration

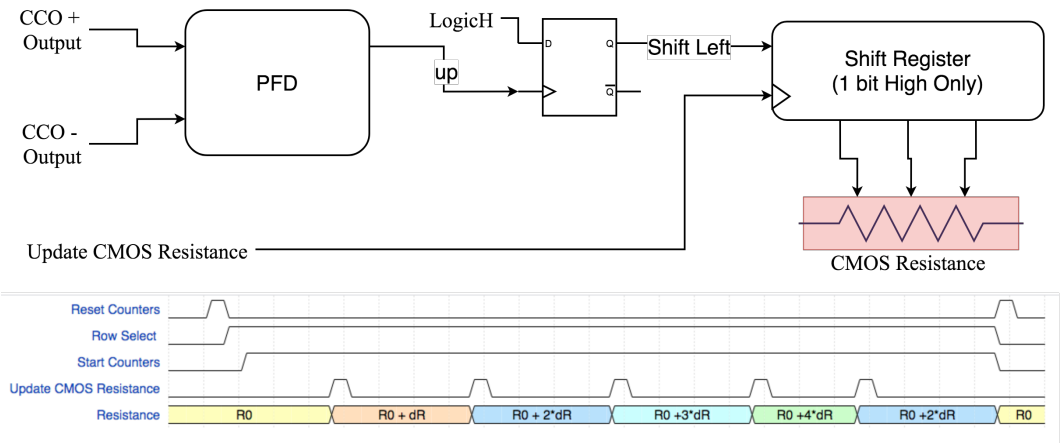

Figure 4.21 CMOS resistance update mechanism of closed-loop self-heating calibration control

time for an imager of 384×288 array size at 30 fps operation. The sensitivity of the channel and the NETD values are calculated by using the sensitivity approach given in [18].

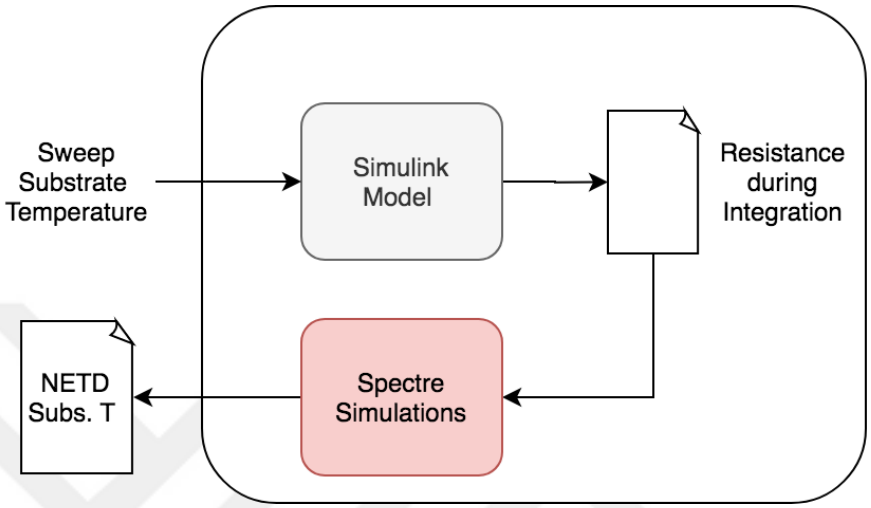

Figure 4.22 Simulation flow of self-heating calibration algorithms

Figure 4.23 reveals that 30 to 40 mK NETD change and a maximum of 400 count difference can be obtained for a substrate temperature change of 10K. The limited difference at the counter outputs over substrate temperature variations suggests that the calibration algorithm forces the oscillators to work in the linear region. The oscillation of the counter output values with respect to substrate temperature might be further decreased if the CMOS resistance update frequency increases. The proposed approach uses row-level blind microbolometer pixels for calibration and offset reduction. The difference of resistance between the blind pixel and the active pixels might cause the readout channel oscillator to operate in saturation. In order to model the effects of resistance non-uniformity to the performance, the Simulink model of pixel resistance between $\pm 5\%$ of the nominal resistances is fed to the Spectre simulations. The simulation results show that the proposed approach can be used up to a resistance non-uniformity of around $\pm 1\%$.

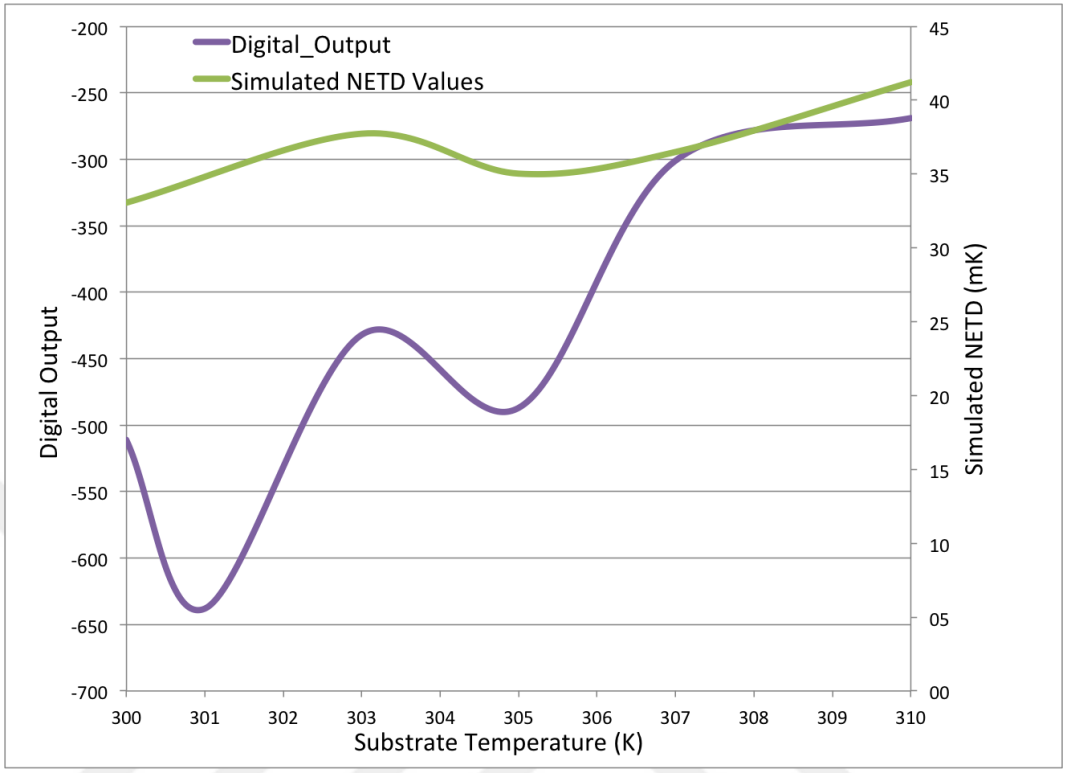

Figure 4.23 Simulation results for closed loop self calibration algorithm

4.8 Conclusion of Chapter 4

This chapter describes the test circuit of the VCO-based microbolometer readout architecture. Test circuit utilizes 4×4 pixel array structure and 1-row reference pixel structure in order to model array effects. Test circuit also connects one active pixel resistor and one reference pixel resistor to IOs, enabling testing the performance of proposed architecture with actual microbolometer resistances. Test circuit also implements bias generation block, serial programming interface, and digital blocks. Last but not least, the test circuit implements a column readout circuit with two-oscillator structures, one for high gain applications and one for high dynamic range applications.

This chapter also mentions the self-heating calibration methods. 2 types of self-heating calibration methods are open-loop calibration with CMOS resistance and closed-loop calibration with CMOS resistance. Closed-loop calibration methods

utilize blind microbolometer pixels and require no bias correction scheme. Thus, the image acquisition logics are simplified, and hence the digital electronics can be minimized. Besides, the proposed architecture also enables TECless operation without the need for calibration look-up tables.

This chapter also shows the layout of the test circuit. Unlike the conventional readout circuit with high area integration capacitances, the column readout circuit utilizes a minimal area, which enables building large frame format imagers. Besides, the proposed architecture requires low supply voltage and dissipates less power compared with the conventional architecture.

CHAPTER 5

MEASUREMENTS and RESULTS

This chapter explains test setup, test firmware and shows test results of the manufactured IC. The test IC has been manufactured in TSMC 65 nm via the Europractice mini ASIC program. This program allocates 2 mm $\times$ 2 mm area to each user. We have designed and produced four different designs to occupy this area effectively. Figure 5.1 shows the manufactured test chip. As can be seen from the figure, there are 2 LC oscillator test circuits, 1 LFSR test circuit, and 1 VCO-based ADC readout test circuit. Figure 5.2 shows the zoomed view of the VCO-based ADC test circuit. The ring structures in this figure show the power routing, namely 1.2 V analog power, 1.2 V IO power, 0.9 V digital power, and 1 analog and 1 digital ground rails. There is also an on-chip capacitance array below the power ring. Test circuits are inside the power rails, but the details could not be seen because of the top metal filling. Some of the dies are packaged with the QFN64 package at IMEC. All of the test results are obtained with the packaged products.

This chapter shows the measurement and test results of VCO based readout architecture. Section 5.1 explains the test setup, firmware and software. Section 5.2 discusses test results of the digital interface and internal circuits, and Section 5.3 shows electrical performance of the Test IC. Finally Section 5.4 concludes this chapter with a summary.

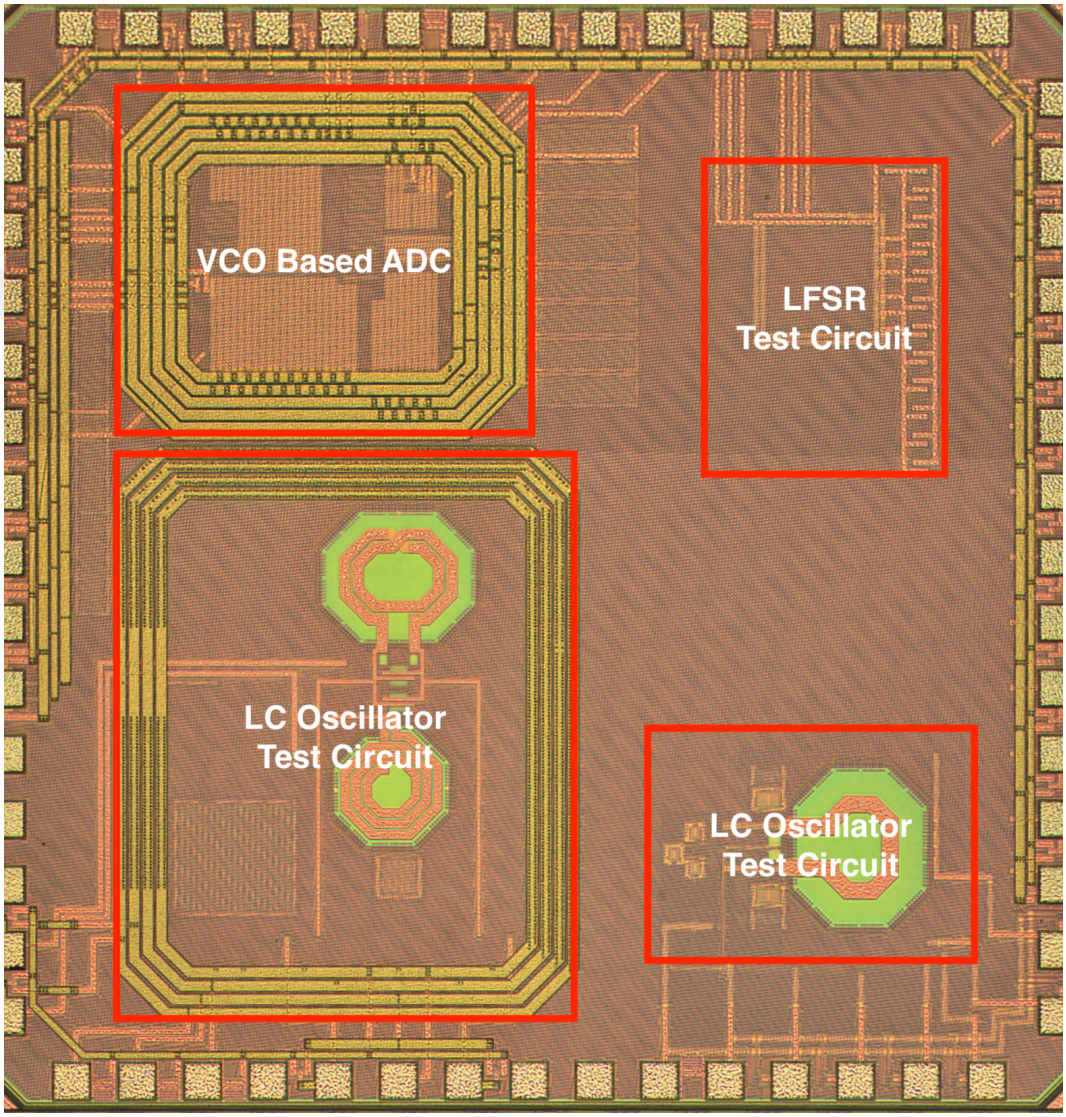

Figure 5.1 Die Photo with all test chips

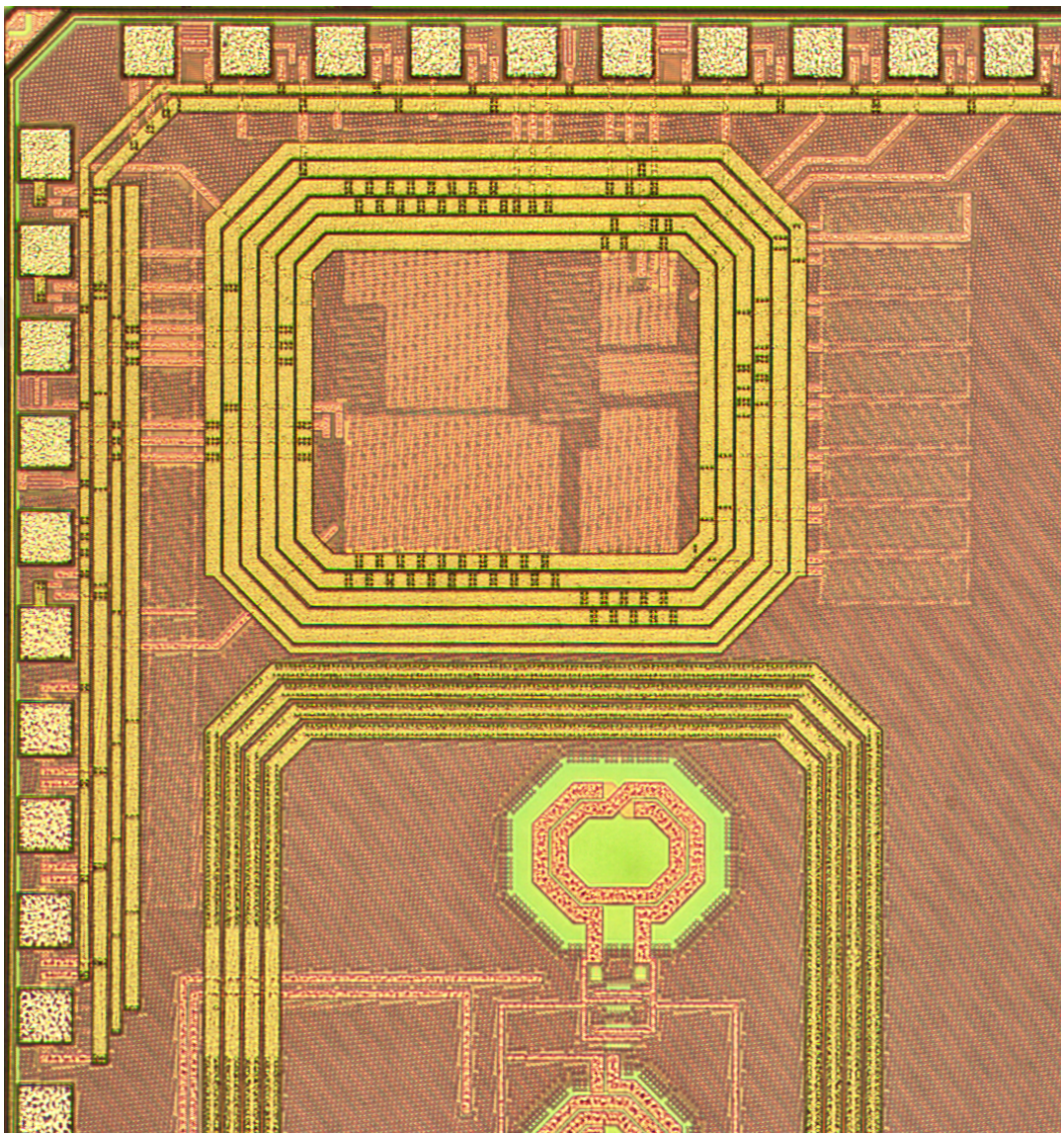

Figure 5.2 VCO based microbolometer readout test circuit in test chip

5.1 Test Setup

This section reviews the test setup, firmware, and software. The QFN64 packages are soldered on top of the commercially available QFN64 to DIP converters, given in Figure 5.3. The prototype circuit is tested by making the connections through the male pins of this product. Besides, external capacitances are connected between the analog and digital power and ground rails.

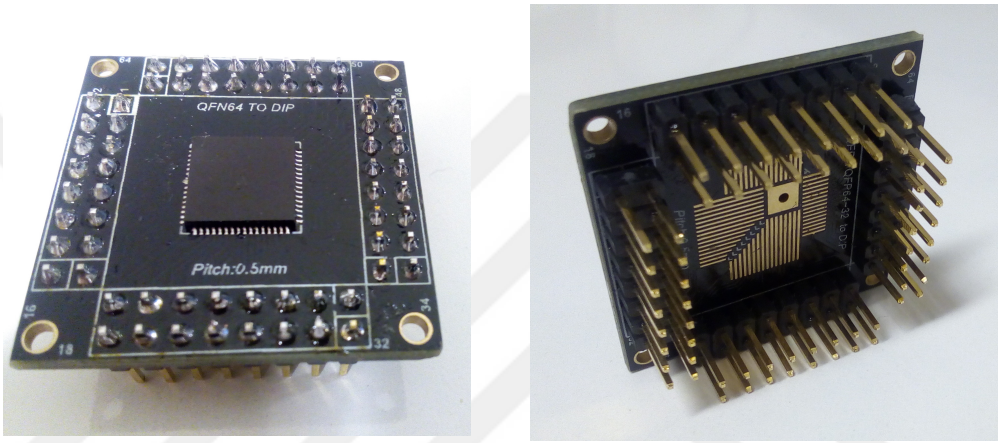

Figure 5.3 Packaged test Ics on the commercial QFN to DIP converter board

Figure 5.4 show the test setup for the performance measurement, which consists of QFN64 to DIP converter, level shifters, Zybo Z7 FPGA demo board, and digitally programmable resistances. The VCO-based microbolometer readout test circuit mainly requires 1.2 V and 0.9 V power supplies and interfaces with the FPGA through the 1.2 V CMOS logic level. Digital programming signals are converted to 3.3 V FPGA logic levels via commercially available uni-directional level shifters. Therefore, all of the digital inputs and outputs are connected to the level shifters before connecting to the FPGA. Pixel and reference resistor IO connections are connected to the programmable resistance for microbolometer performance testing. These nodes are arranged to be driven with an external voltage supply to measure the performance of the VCO-based ADC with respect to the input voltage. The pixel and reference biases are disabled in this configuration, and the column readout circuit is driven from the external pixel and reference pads.

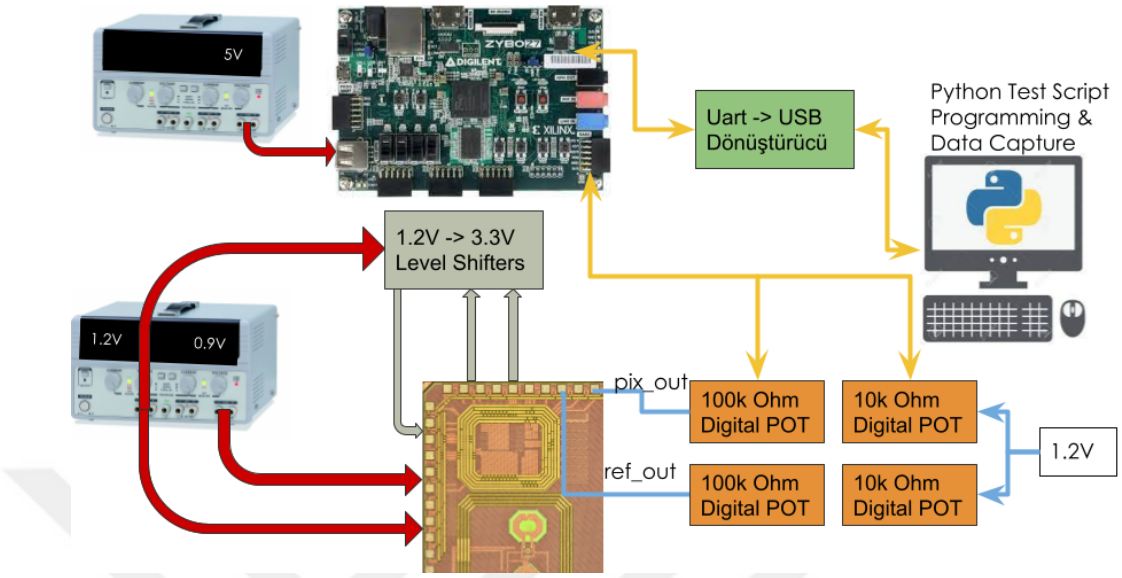

Figure 5.4 VCO based microbolometer readout circuit performance measurement test setup

Test firmware consists of 3 components, programming interface, data capture, and data release to the computer. Figure 5.5 shows the block diagram of the test FPGA firmware. Test firmware mainly gets the commands from the computer via the UART interface and conveys them to the command interpreter block. This block drives either the test chip SPI drivers or the digitally programmable POT's SPI drivers. The test firmware also captures the serially driven digital outputs of test IC and converts them to 13-bit parallel data. This section also tags the data with the row and frame number info. Labeled data is recorded on the asynchronous FIFO to drive the digital outputs from the UART Tx interface. Last but not least, test firmware produces necessary clocks for the SPI drivers and UART controller.

The test software is responsible for capturing the output data and programming the test IC and digitally programmable resistances. Test software captures the data from all of the channels and creates the statistics of the data with the given sample times. This software is written in Python, and performance metrics are obtained via the Python Statistics library. The software can also set the number of rows and number of samples and it can create records and graphs for all rows and columns separately.

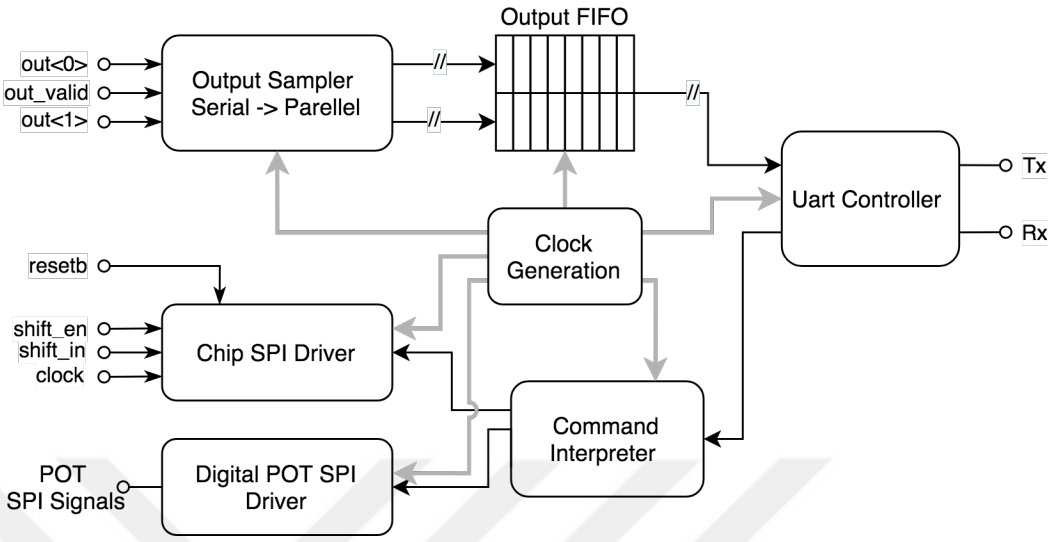

Figure 5.5 Block diagram of the FPGA Firmware

5.2 Digital Results

This section shows the digital test results of the IC. First of all, the serial programming interface is tested. In this test, serial programming input signals are driven from the FPGA, and the test output pin is observed from the oscilloscope. Figure 5.6 shows the oscilloscope view of the serial programming interface test, including *shift_in*, *shift_en*, *shift_clock* inputs, and *shift_out* output. The IC is programmed by driving the *shift_in* input "0110 1010 1011 0101" while *shift_en* is asserted. At this point, *shift_out* signal remains silent. When the second programming occurs, digital test output pin (*shift_out*) shows the inverted version of the first programming sequence. The inversion occurs since the FPGA buffers, converting the signal level from 0.9 V to 1.2 V, inside the chip is designed to be in an inverting manner. This test shows that the programming interface works as expected.

The second test for validating the serial programming interface shows the memory inside the chip works as intended. For this purpose, *digtest* pad is programmed to show the *frame_start* and *row_start* signals, respectively. Test firmware changes the line time and the number of rows to verify the programmability and functionality of the memory. Figure 5.7 shows the oscilloscope view of the *frame_start* and *row_start* signals. In Figure 5.7a, the number of rows is programmed as 2, and line time is

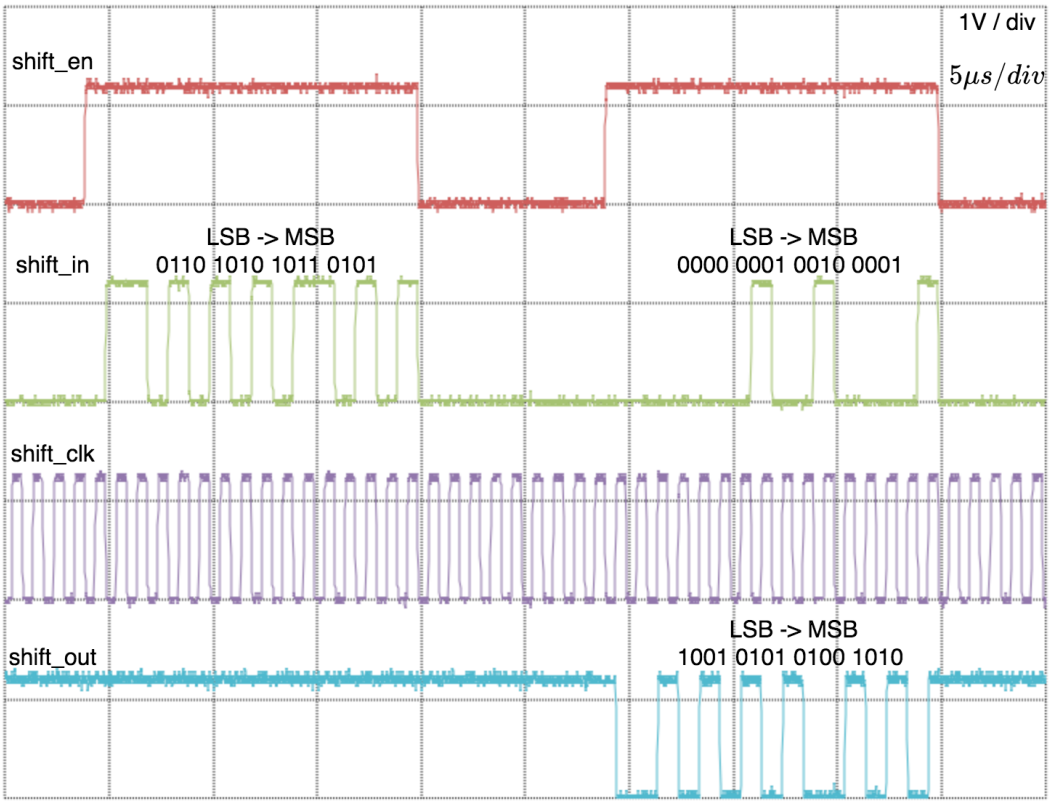

Figure 5.6 Serial programming signals oscilloscope view with 1V/div and 5μs/div settings

programmed as 20 cycles, changing from 100 (default value). This means that the frame includes two rows with a line time of 20 μs for 1 MHz input clock. Figure 5.7b shows the oscilloscope view when the number of rows is changed to 8. The oscilloscope views show that the memory array can be programmed as intended. This test is extended to cover all of the memory bits, and no-fault has been detected.

The third test tries to show that the oscillators work as expected. For this purpose, the digital test output pin is programmed to drive the counter test output, which is one-fourth of the oscillator output signal, and *ring_start* signals for two oscillator structures. Figure 5.8 shows that the oscillation starts after the *ring_start* signal for both configuration. This figure also shows that the oscillation frequency of the 3-stage configuration is higher than the oscillation frequency of the 5-stage configuration, as expected.

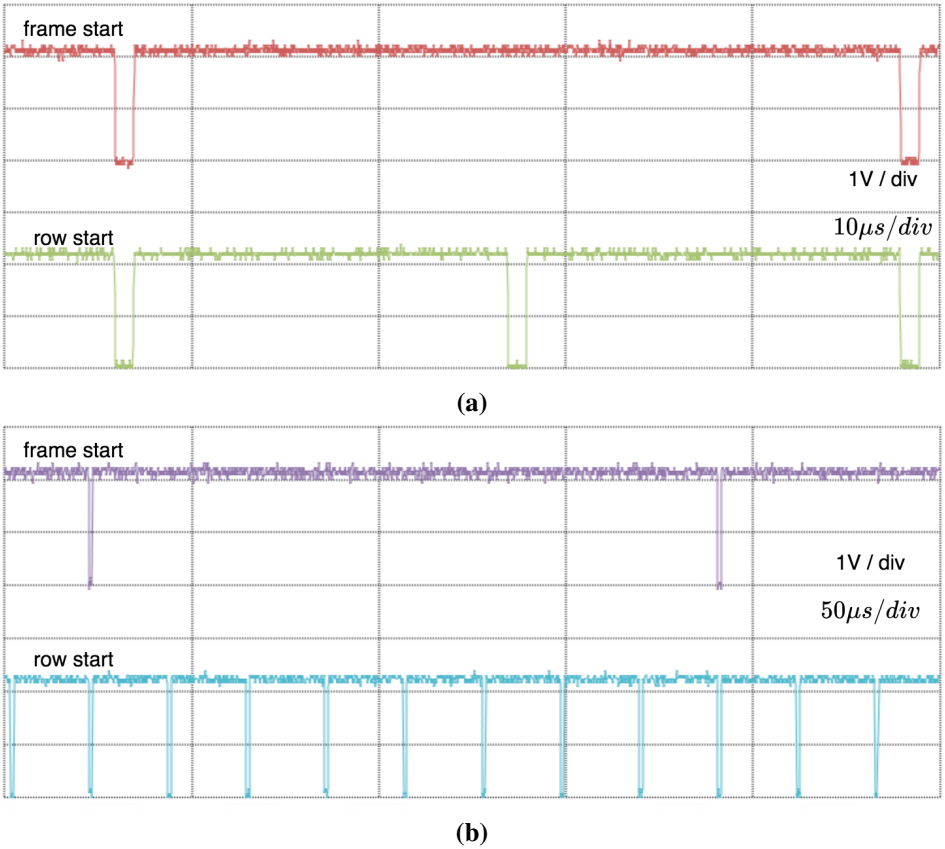

Figure 5.7 Frame and row start signals when number of rows is programmed as (a) 2 and (b) 8

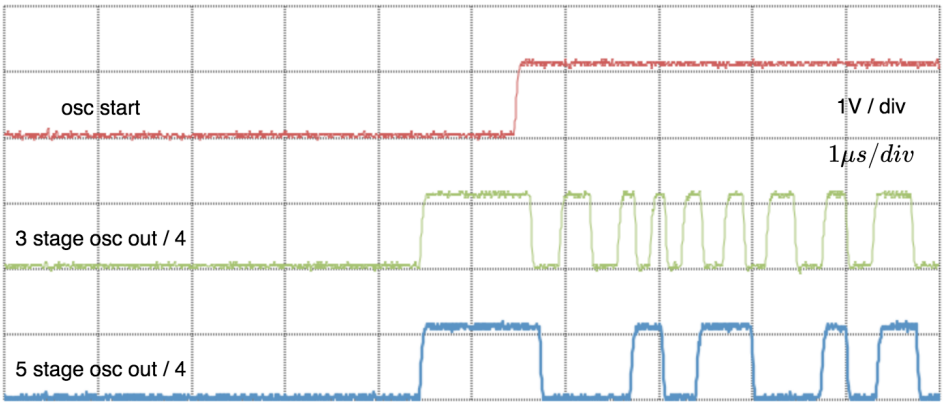

Figure 5.8 One forth of oscillator outputs waves for both 3 stage and 5 stage ring oscillator configurations with oscillator start signal

5.3 Electrical Performance

First, the bias generator of test IC is tested by using a multimeter. The bias voltage of the Widlar current generation block yields a voltage level similar to the simulations. The master current value is monitored by connecting a resistance from the current test point to the analog supply voltage. The initial measurements show that 10 μA master current is driven from the Widlar current generation block. This measurements show that the bias generation block works as intended.

Then, the VCO-based column readout circuit is tested to analyze the performance of the proposed architecture. To be able to explore the performance metrics, this section is divided into four parts:

- Gain results capture the counter outputs with respect to applied dc voltage and connected resistance values.
- Noise results show the noise performance of the circuit with different input configurations.
- Sensitivity analysis is carried out combining gain and noise results,
- Calibration methods are tested via an external signal generator.

5.3.1 Gain Results

This section analyzes the performance of the VCO-based column readout in two ways; the first one is obtained when the inputs are driven from the external supply, the second one is obtained by changing the resistances of digitally programmable resistances.

The gain of the proposed architecture (Counts/V) is obtained with respect to applied voltage bias for the first gain analysis. For this configuration, the pixel and reference bias circuits are disabled, and the test circuit is configured as a 1-row circuit. The gain from the input voltage to the digital output is obtained by changing the differential input voltage on top of the dc bias voltage. The dc voltage of the inputs is selected as 300 mV, which is the default voltage value when a 60 kΩ resistances is connected.

The differential voltage is applied from the pads of the test circuit, and the counter outputs are recorded for 100 μs sampling (i.e., integration) time. The same setup is used to capture the digital outputs when the test circuit is programmed to work with 3-stage and 5-stage oscillators. Figure 5.9 shows the counter outputs with respect to applied differential voltage for both of the oscillator configurations. This figure shows that both oscillator configurations yield linear gain between $\pm$10 mV input voltage difference, whereas the non-linearity of the oscillators becomes dominant outside of $\pm$10 mV input voltage region.

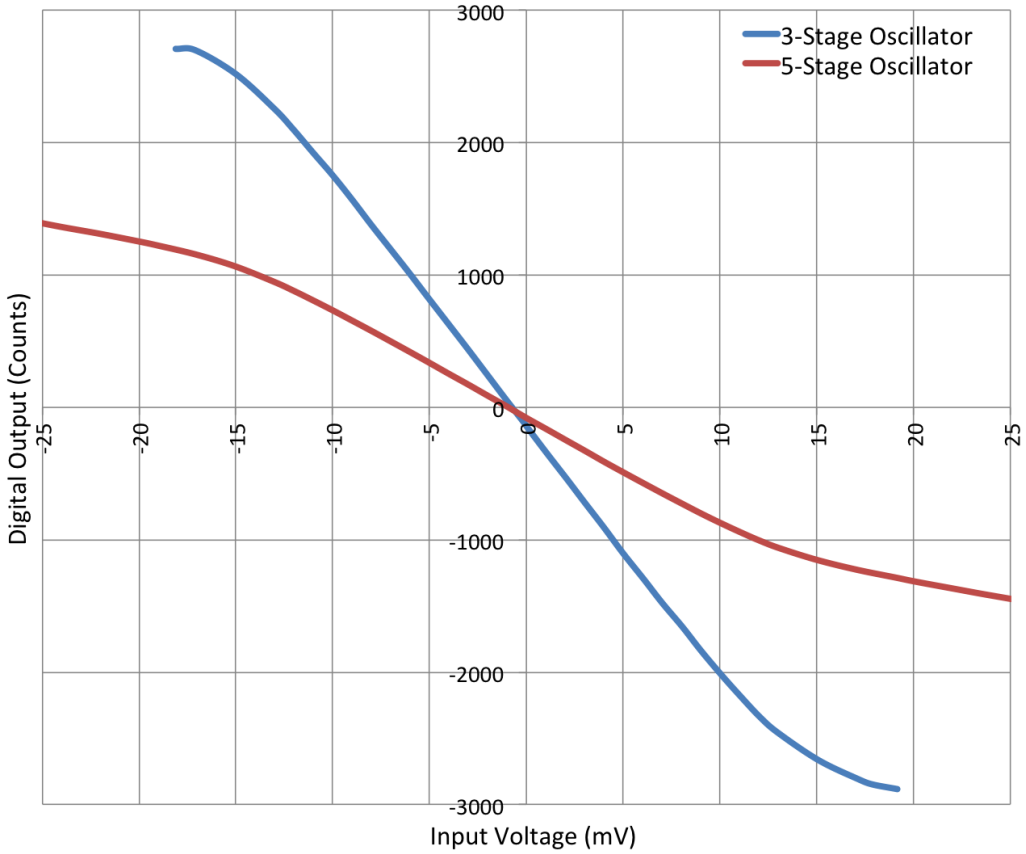

Figure 5.9 Digital output with respect to differential input voltage for 3 and 5 stage ring oscillators

Figure 5.10 shows the gain of the architecture in terms of Counts/mV for 3-stage and 5-stage oscillator configurations. The architecture yields 182 Counts/mV and 82 Counts/mV gains for 3-stage and 5-stage oscillator configurations, respectively in $\pm$10 mV input intervals. The gain of the 3-stage configuration is more than twice of

the 5-stage oscillator configuration. Besides, the gain of the architecture drops to reasonable points when the input voltage difference is between $\pm$10 mV to $\pm$20 mV. These regions correspond to high temperature in microbolometer readout architecture. This gain decrease can be useful when looking into high-temperature objects for presence detection. In classical architecture, the integration capacitances easily saturate when high-temperature objects are at the scene. However, this architecture enables to differentiate the objects from the scene with the help of gain degradation at the edges of dynamic range.

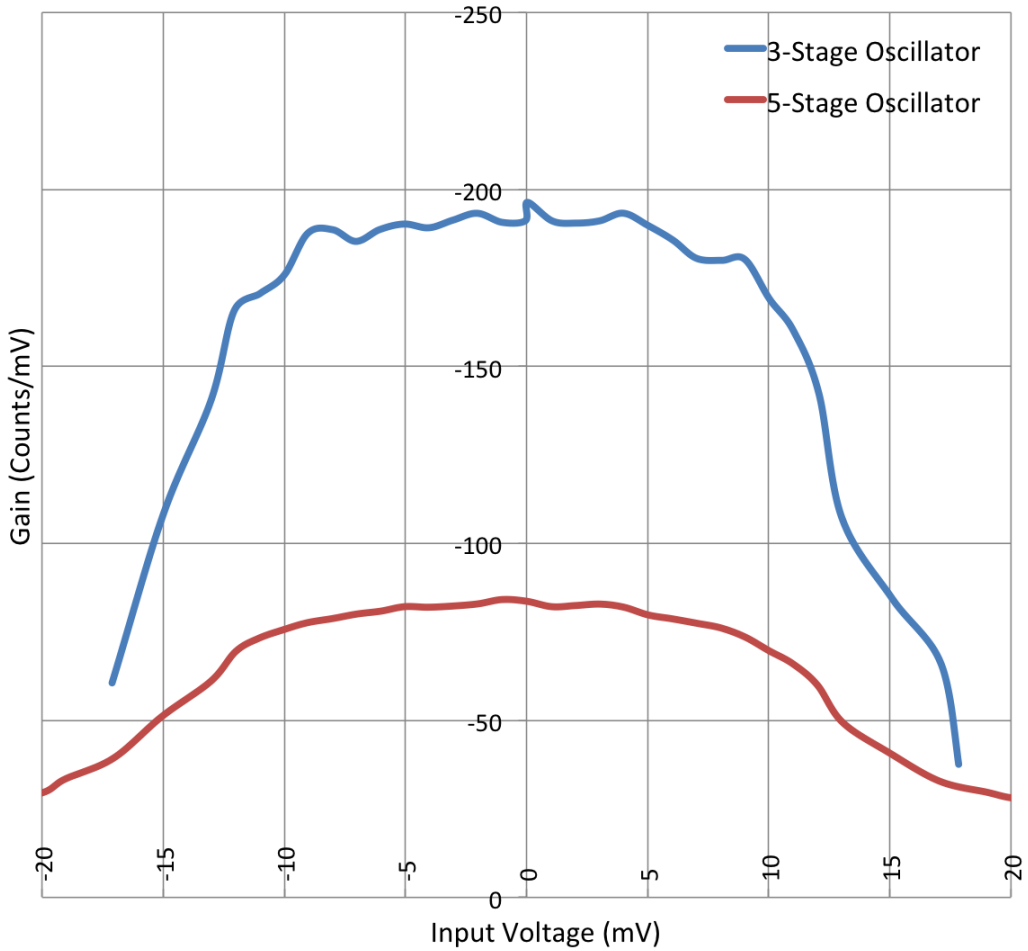

Figure 5.10 Gain of the structure with respect to differential input voltage for 3 and 5 stage ring oscillators

The second gain measurement test tries to capture the gain of the architecture in terms of Counts/Ω. For this purpose, the pixel and reference biases are activated,

and the resistance values of the digitally programmable resistances are changed. Two resistances of 60 kΩ nominal resistance value are connected to both pixel and reference nodes. The resistance difference between these two nodes is swept from -1500 Ω to +1500 Ω. Figure 5.12 shows the counter outputs with respect to pixel and reference resistance differences for both 3-stage and 5-stage oscillator configurations. This figure shows that ±700 Ω resistance difference yields linear gain for both 3-stage and 5-stage structures.

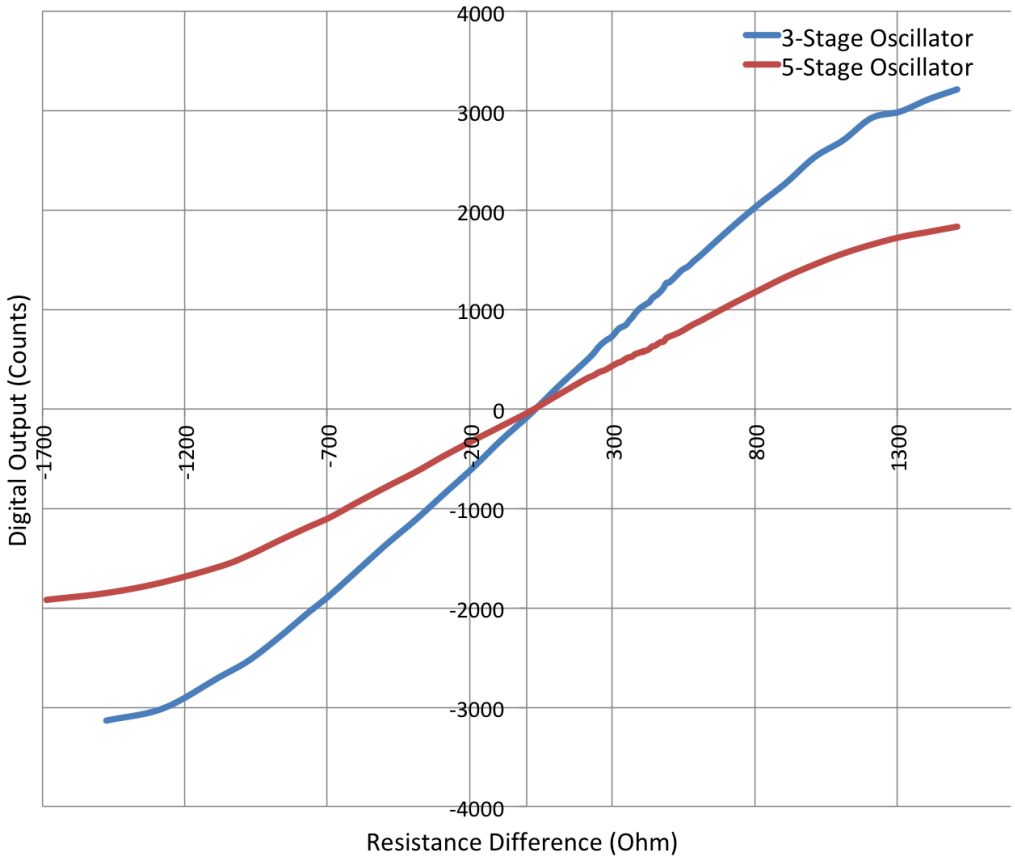

Figure 5.11 Digital output with respect to resistance difference

To further investigate the linearity, the gain with respect to resistance difference curves is obtained. Figure 5.12 shows the resistive gain of the architecture. As can be seen from the figure, 3-stage oscillator configuration yields more than 2.5 Counts/Ω whereas 5-stage oscillator configuration yields 1.5 Counts/Ω gain in the linear region. This figure also shows that the 5-stage oscillator configuration yields linear gain between -800 Ω and +700 Ω, and the 3-stage oscillator configuration yields linear

gain -700 Ω and +500 Ω. This corresponds to scene dynamic range of 83 °C, and 66 °C respectively, for 25 μm microbolometer structure of parameters given in Table 2.1. The digitally programmable resistance has large step sizes and a high percentage of uncertainties, resulting in the fluctuations of the gains at the linear region.



Figure 5.12 Gain of the structure with respect to resistance difference for 3 and 5 stage ring oscillators

5.3.2 Noise Results

The proposed architecture is also analyzed in terms of noise to calculate the architecture's sensitivity. The noise performance of the circuit is measured by calculating the standard deviation of the digital outputs with 5000 samples. Two different setups

are created, and the noise performance of the sub-circuits is measured. First, the noise performance of the VCO-based column readout is measured. For this purpose, the pixel biases are disabled, and test IC is programmed to work as a 1-row imager. In this configuration, pixel and reference nodes are shorted to eliminate the noise components due to voltages. Figure 5.13 shows the counter output histogram of this setup for 3-stage oscillator configuration. This histogram yields 1.2 Counts of standard deviation, i.e., output noise. This noise yields approximately 6.6 μV_{rms} input-referred noise. This noise value equals the 0.44 Ω resistance when biased with 15 μA of constant current. 5-stage oscillator configuration yields 0.8 counts of standard deviation, yielding 4.4 μV_{rms} input-referred noise. This input-referred noise equals to 0.29 Ω resistance when biased with 15 μA of constant current.

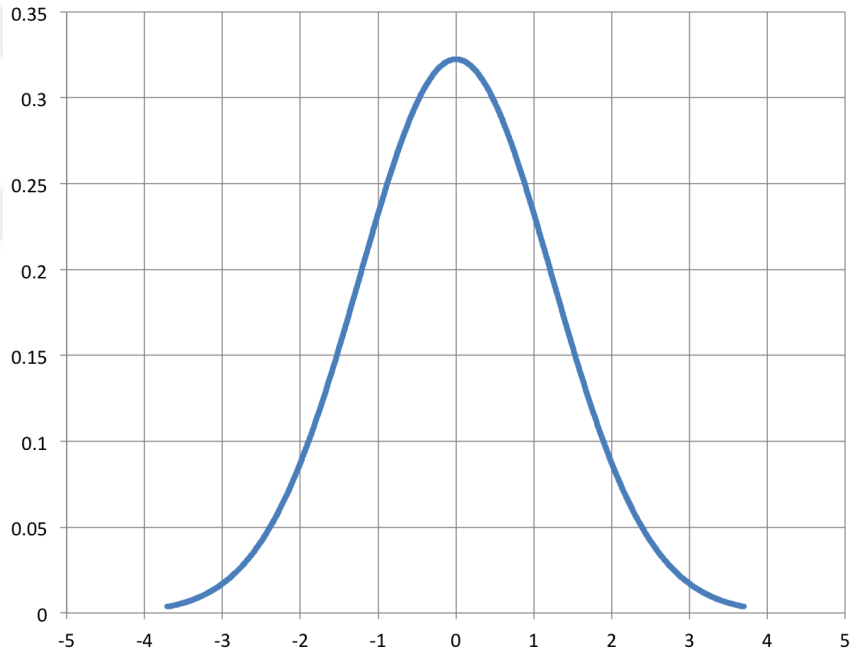

Figure 5.13 Output histogram when input shorted yielding 1.2 counts standard deviation

The second setup tries to measure the noise performance of the system when all the components are in place. For this purpose, the pixel and reference current bias circuits drive external 60 kΩ resistors. Therefore, this setup includes the noise of bias circuits and resistors. Figure 5.14 shows the digital output histogram of this setup for the 3-stage ring oscillator configuration, including bias generation and

external resistors. The standard deviation of the digital output histogram is calculated as 2.6 counts, which yields approximately 14.3 μV_{rms} input-referred noise. This input-referred noise equals 0.95 Ω of input resistance when biased with 15 μA of constant current. 5-stage oscillator configuration has a 1.7 counts standard deviation, yielding 9.3 μV_{rms} input-referred noise. This input-referred noise equals 0.62 Ω of input resistance when biased with 15 μA of constant current. This means that the noise component of bias generation and pixel resistance is 12.7 μV_{rms}. The noise increases significantly when the bias circuits and the pixel circuits are connected. Therefore, the system noise can also be further decreased by implementing a low noise bias generation circuit and implementing a chopping filter between the pixel and transconductance amplifiers.

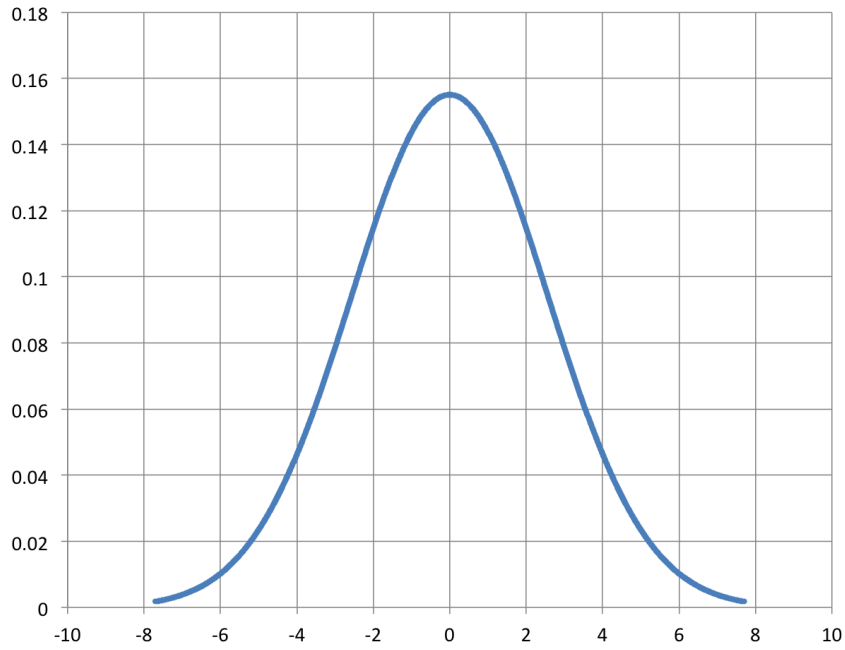

Figure 5.14 Output histogram of the readout circuit driving external resistances yielding 2.6 counts standard deviation

5.3.3 Sensitivity Analysis

The performance metric of the microbolometer infrared imagers is measured in terms of noise equivalent temperature difference (NETD). The calculation of the NETD as a parameter of resistance sensitivity is analyzed in Chapter 2. The NETD

performance of the proposed architecture is calculated by combining the gain of the structure, $A_{readout}$, and standard deviation of the system, $\sigma_{readout}$, with the infrared to resistance conversion gain, A_{ir}, given in Table 2.1 as 100 mK / 1.8 Ω. NETD of the system is calculated as

$$NETD = \frac{A_{readout} * A_{ir}}{\sigma_{readout}}. \quad \textbf{(5.1)}$$

Figure 5.15 shows the calculated NETD with respect to the pixel and reference resistance difference for the 3-stage ring oscillator configuration. The exact figure also shows the computed NETD values with respect to the calculated scene temperature for the 3-stage ring oscillator configuration. The proposed architecture yields approximately 55 mK NETD, which is slightly higher than state-of-the-art NETD figures [19, 52, 53] for 25 μm pixel pitch microbolometers, in linear gain regions. This NETD figure is obtained only when the noise component of the actual pixel resistance is under 0.9 Ω resistance value, which is the noise component of the system. The dynamic range of the linear area is around 80 K. However, the proposed architecture also yields smaller than 200 mK NETD performance for low gain regions, marked as high dynamic range (HDR) regions. The decrease in the high-temperature areas is a desirable feature for high dynamic range applications. This phenomenon can be called an inherent high dynamic range (HDR) of the proposed architecture. This property is mostly desired when trying to see the details on the high temperature and low-temperature objects at the same time. The gain degradation at high-temperature regions is due to nonlinear voltage to frequency gain characteristics of oscillator structure. This nonlinearity causes a big problem when this architecture is used as a stand-alone ADC circuit. However, this drawback enables implementing HDR operation in infrared imaging applications.

5.3.4 Calibration Method Results

This section gives the measurement result of the proposed self-heating calibration methods using CMOS resistance instead of blind microbolometer resistances. The first method implements a calibration algorithm with an open-loop control of CMOS resistance. To be able to test this method, the pixel bias is disabled and the pixel bias

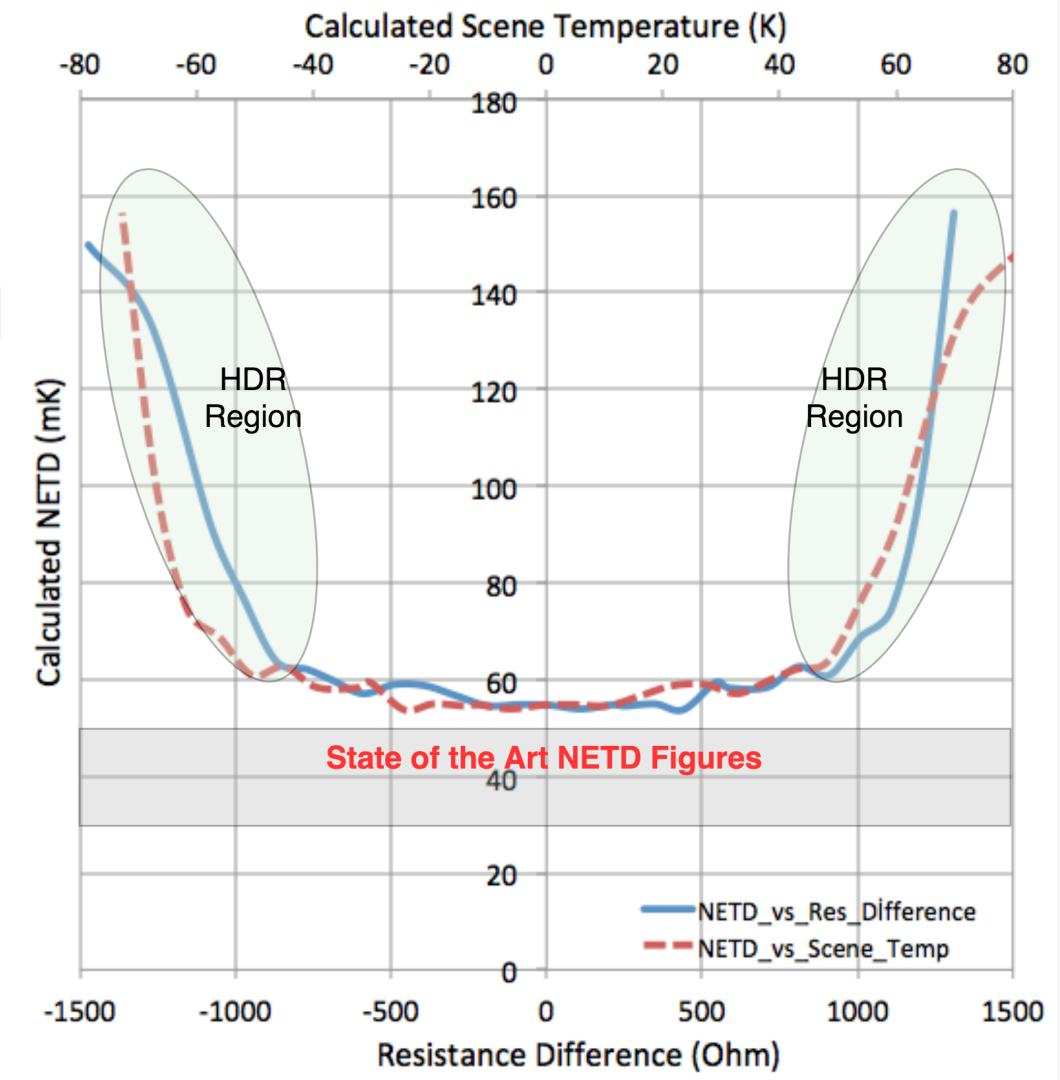

Figure 5.15 Calculated NETD with respect to the resistance difference and calculated scene temperature for $25\mu m$ pixel pitch microbolometer with an $f\#1$ optics

node is driven from the signal source, while the reference node voltage is obtained by biasing the CMOS resistance with a constant current. Figure 5.16 shows the oscilloscope view of the pixel and reference node voltages. In this figure, the blue line shows the start signal of the oscillator structure, the red line shows the pixel output voltage, and the green line shows the reference voltage, which is created by changing the CMOS resistance. When the oscillator start signal is asserted, the green line, on-chip generated reference voltage, increases with a constant slope. This method tries to mimic the voltage change due to self-heating by changing the CMOS resistance step by step at constant time intervals.

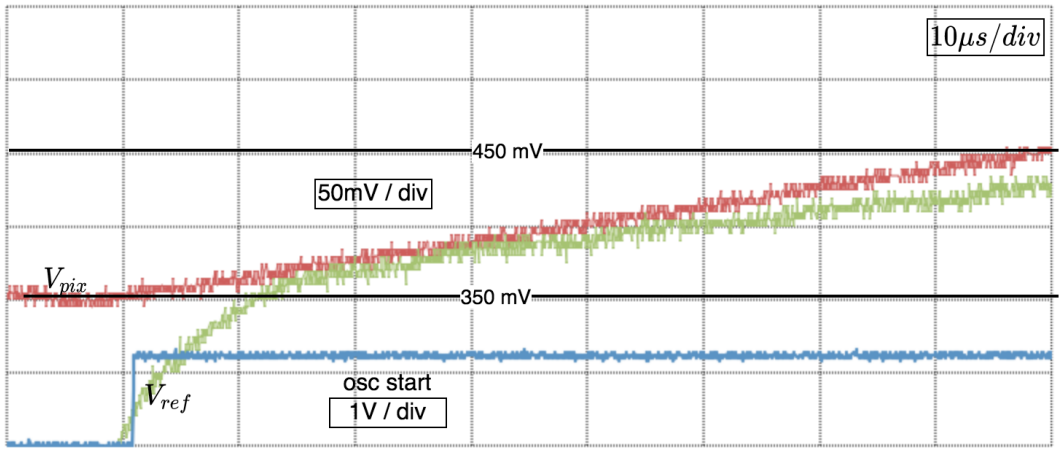

Figure 5.16 Open loop bias calibration test results, including pixel voltage supplied from signal generator and reference voltage generated on-chip

The second proposed method uses blind reference resistance at the calibration channel as mentioned in Section 4.7. To be able to test this method, the pixel bias voltage is driven from the signal source, while the reference voltage is obtained by biasing the CMOS resistance with a constant current source as in the testing of the first calibration method. Figure 5.17 shows the oscilloscope view of the pixel voltage and the reference voltage. In this figure, the blue line shows the start signal of the oscillator structure, the red line shows the pixel output voltage, and the green line shows the reference voltage, which is created by changing the CMOS resistance. When the oscillator start signal is asserted, the reference CMOS resistance is arranged to keep the voltage difference between pixel and reference nodes constant. The reference voltage tries to follow the pixel voltage since the counter output is

sampled and the shift amount of the resistance is decided accordingly. As can be seen from this figure, this method creates lower pixel to reference voltage difference when compared with the open-loop control of CMOS resistance.

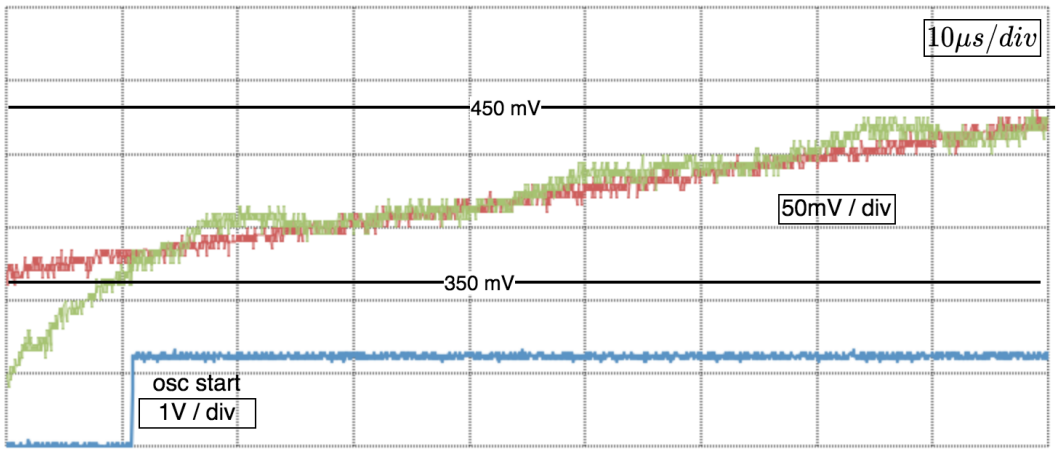

Figure 5.17 Closed loop bias calibration test results, including pixel voltage supplied from signal generator and reference voltage generated on-chip

The effectiveness of the calibration methods should be measured when the microbolometer active and reference resistances are used as loads. The above-mentioned graphs show that the proposed calibration circuit works, and the reference voltage tracks the pixel voltage. The next step to verify the performance of the self-heating calibration algorithms is to try these methods on the actual microbolometer resistors and measure the respected output voltage drift and NETD values. To measure these performance metrics, the microbolometer readout circuit should be produced as a full wafer, and the resistance array should be grown with wafer-level process. However, connecting microbolometer resistor to this test circuit is impossible since it is designed only to validate the effectiveness of the architecture and to test circuit produced in the MPW project.

5.4 Results and Conclusion

The previous section shows the gain and noise measurement results and calculates the respected performance metrics. This section first shows the measurement results

of test IC in terms of power and compares the proposed architecture with the state-of-the-art designs.

The readout channel requires both 1.2 V and 0.9 V DC power supply for the analog and the digital sides of the proposed architecture, respectively. Analog supply provides power to transconductance amplifier and pixel bias circuit, while digital supply provides power to the oscillator, the counter, and the differentiator circuits. The test circuit is configured to disable some of the blocks to measure the power need of the sub-blocks. First, the oscillator start signal is forced to set the oscillator to work in a silent state. The delta current shows the power need of the oscillators, the buffers, and the counters. For this configuration, delta current is measured as 9μA, which yields to 4.5 μA for one channel. Then, the currents driving the transconductance amplifiers are disabled, and the delta current is measured as 18 μA, resulting 9 μA current dissipation per channel. The pixel and reference currents are measured from the external resistances as 14 μA. For the single row of operation, the analog supply demands a total of 37 μA of current, whereas the digital supply demands a total of 4.5 μA of current. This results in total of 48 μW power dissipation per channel.

A power consumption per channel value (Power/Channel) is calculated as in [52] to compare the power consumption with the previous works. The prototype integrated circuit is manufactured and the actual power consumption is measured on the hardware to validate the proposed architecture. In [52], 10 mW power consumption is reported for I/O and the digital circuits for a 320x240 array format, which adds up as 31.25 μW power consumption to the single channel. As a result, the power consumption per channel for the proposed architecture is calculated as 79 μW.

The proposed architecture occupies a small area when compared with the conventional readout architectures. In order to compare with the published works in terms of the layout area, the readout array layout area per pixel area is calculated. The readout layout area metric (ChArea/PixArea) of the published works, [19, 53], is calculated by comparing the pixel area to the column area from the corresponding micrographs of the published results. Their ChArea/PixArea values are higher than 100, while the proposed readout architecture needs only 8 pixels area for a single channel.

Table 5.1 compares this work with the state-of-the-art works in terms of 5 different properties. NETD metric is not given in Table 5.1 because of the fact that two of the published works are designed as imagers, while this work and the work in [52] is intended to be test circuits. The proposed architecture yields slightly worse NETD performance dissipates lower power and occupies a smaller layout area. This work can be classified as an all-digital approach, while the previous works use an analog-driven approach that requires high voltage headroom to get the desired SNR. This all-digital column readout needs to be manufactured in 65 nm or smaller technology nodes to get the desired performance since unit delays decrease with decreasing feature size. All-digital readout architecture also enables implementing digital correction circuits on-chip with lower power consumption and higher flexibility.

Table 5.1 Comparison with the state of the art

	This work	**[52] 2020**	**[53] 2014**	**[19] 2014**
ROIC	VCO based	TDC based	Analog w multi bolos	CTIA based
Process	65 nm	130 nm	350 nm	180 nm
Supply	1.2 V	1.2 V	5 V	3.3 V
Power/Ch[a]	79 μW	81 μW[b]	457 μW	220 μW
Pitch	25 μm	17 μm	25 μm	25 μm
ChArea/PixArea[c]	8	16	>100	>100

[a] Total power is normalized to number of readout channels.
[b] The paper reports 66 μW, but the power is miscalculated.
[c] This metric is derived from the layout view of the published works.

CHAPTER 6

CONCLUSION

The research conducted in this thesis focuses on designing a low voltage and low area microbolometer readout circuit. The main target of this study is to propose a new architecture to enable designing large frame format FPAs with lower power consumption. To catch up with this goal, voltage-controlled oscillator (VCO) based readout architecture is introduced. This architecture uses the integration property of the oscillator instead of implementing a commonly used CTIA based integrator. The proposed architecture eliminates the need for large voltage supply and large capacitances of classical microbolometer readout circuits. The almost-digital property of the new architecture enables the implementation of large FPAs with lower power consumption. In order to validate the operation of the proposed architecture and compare its performance to the other architectures in literature, a prototype test circuit is designed and fabricated at TSMC 65 nm CMOS process node. The measurement results show that the proposed architecture yields performance results comparable to the state-of-the-art microbolometer readout architectures while it achieves significantly lower power dissipation with a considerably smaller layout area. In the following, the improvements of the proposed architecture is listed if the new architecture is used as a microbolometer readout circuit in a focal plane array (FPA):

1. The proposed architecture both integrates and converts the microbolometer pixel outputs at the same time. In this way, it eliminates the need for an external analog to digital converter.

2. The power consumption can be reduced to one-third of the classical microbolometer readout architecture with an additional analog to digital conversion property.

3. The column readout area can be reduced to one-tenth of the classical microbolometer readout architecture. The reduction in layout area enables producing the higher resolution FPAs.

4. The performance measurements show that this architecture can provide 55 mK NETD values with a reasonably high decrease in power consumption.

5. The new architecture enables implementing different self-heating calibration methods implementing CMOS resistances. Two of these methods are proposed in this study. The simulation results show that both of these methods yield good performance results.

6. The proposed architecture requires to be manufactured in higher precision technology nodes (lower than 65 nm feature size) to obtain required VCO gains. Low feature size technology nodes enable on-chip implementation of digital correction algorithms.

The prototype readout circuit developed in this thesis has been electrically tested in great detail to verify its functionality and to determine its performance parameters. Test results showed that two areas could be improved in further works. First, the bias generation scheme should be made supply and temperature independent. In order to decrease the bias-related noise sources, the pixel and reference bias currents should be generated from the same source. Second, the chopping filter should be implemented in the column readout circuit to decrease the high-frequency noise components of the pixel resistances and bias circuits. Based on the results obtained in this thesis, it has been concluded that requiring several areas need further research and study as summarized below;

1. The readout architecture, bias generation, and column readout should be revised to eliminate the high-frequency noise components.

2. The readout architecture can be designed to provide its powers internally and level shifters could be implemented on-chip.

3. The readout architecture should be designed for a complete focal plane array (FPA). The microbolometer pixel and reference pixel structure should be grown on top of the designed readout circuit. The complete imaging structure should be tested under vacuum conditions (thermal isolation from the surrounding environment) to validate the performance as an infrared imager.

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